INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

“To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates.”

DEPARTMENTAL MISSION

“Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool”.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM OUTCOMES(POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainble development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and mangement principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sr.No.	Name of the Faculty	Activities
1	Prof. S. B. Akkole	GATE / Preplacement Coaching
		ED Lab Incharge
		Students Mentor
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		Participation in Funded Projects
2	Dr. R. R. Maggavi	GATE / Preplacement Coaching
		CN Lab Incharge
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub COordinator
		NBA Criteria Coordinator
		Innovations Club Coordinator
3	Prof. S. S. Malaj	GATE / Preplacement Coaching
		Adv.Comm. Lab Incharge
		Students Mentor
		Dept. NAAC Criteria Sub COordinator
		NBA Criteria Coordinator
		NIRF Coordinator
		Conference Coordinator
04	Prof. S. S. Kamate	GATE / Preplacement Coaching
		VLSI Lab Incharge
		Students Mentor
		Module Coordinator
		IEEE Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		Project Coordinator
05	Porf. D. M. Kumbhar	GATE / Preplacement Coaching
		AC Lab Incharge
		Students Mentor
		Dept. Association Coordinator
		Class Teacher
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Dept. ED Cell Coordinator
06	Prof. S. S. Patil	GATE / Preplacement Coaching
		ARM & ES Lab Incharge
		Students Mentor
		Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Admission Coordinator
		Module Coordinator

CONTENTS

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	10	15.76Y
2	Technical supporting staff.	03	21.02Y
3	Helper staff	02	20.50Y

MAJOR LABORATORIES

S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	35.51
2	Analog Electronics (ED &I) Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.50	7	Research/E-Yantra/DSP & C.N.Lab	71	16.49
4	HDL/MC / EMD Lab	71	19.57	8	Power Electronics Lab	--	4.86
Total Investment In The Department						**Rs. 95.31 Lacs**	

FACULTY DETAILS

TEACHING FACULTY

S.N.	Name and Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Dr. R. R. Maggavi	Ph.D	E&C	LMISTE	17Y.05M	9480275583
2	Sri S B Akkole	M.Tech.	Communication	LMISTE	27Y.03M	9480422508
3	Smt.S.S.Kamate	M.Tech	Digital Electronics	LMISTE	19Y.00M	9008696825
4	Smt. S. S. Malaj	M.E.	E & TC	LMISTE	24Y.07M	9731795803
5	Sri. D.M. Kumbhar	M.Tech	Electronics	LMISTE	17Y.10M	09373609880
6	Sri. Sachin .S. Patil	M.Tech	VLSI & Embedded	LMISTE	17Y.08M	9448102010
7	Sri .D.B. Madihalli	M.Tech	Industrial Electronics	LMISTE	14Y.07M	9902854324
8	Sri.P.V.Patil	M.Tech	VLSI & Embedded	LMISTE	9Y.04M	9731104059
9	Sri.S.S.Ittannavar	M.Tech	DSP	LMISTE	8Y.11M	9964299498
10	Smt. B. P. Khot	M.Tech	Microelectronics & Control Systems	LMISTE	5Y.11M	9964019501

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience (in years)
1.	Sri. P. S. Desai	DEC	21Y-.07M
2.	Sri. V. V. Guruwodeyar	DEC	30Y-02 M
3.	Sri.M.A.Attar	DEC	11Y-09M

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

III SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	BSC	18MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	--	03	40	60	100	3
2	PCC	18EC32	Network Theory		3	2	--	03	40	60	100	4
3	PCC	18EC33	Electronic Devices		3	0	--	03	40	60	100	3
4	PCC	18EC34	Digital System Design		3	0	--	03	40	60	100	3
5	PCC	18EC35	Computer Organization & Architecture		3	0	--	03	40	60	100	3
6	PCC	18EC36	Power Electronics & Instrumentation		3	0	--	03	40	60	100	3
7	PCC	18ECL37	Electronic Devices & Instrumentation Laboratory		--	2	2	03	40	60	100	2
8	PCC	18ECL38	Digital System DesignLaboratory		--	2	2	03	40	60	100	2
9	HSMC	18KVK39/49	Vyavaharika Kannada (Kannada for communication)/	HSMC	--	2	--	--	100	--	100	1
		18KAK39/49	Aadalitha Kannada (Kannada for Administration)									
		OR										
		18CPC39/49	Constitution of India, Professional Ethics and Cyber Law		1	--	--	03	40	60		
					Examination is by objective type questions							
				TOTAL	17 OR 18	10 OR 08	04	24 OR 27	420 OR 360	480 OR 540	900	24

Note: BSC: Basic Science, PCC: Professional Core, HSMC: Humanity and Social Science, NCMC: Non-credit mandatory course.

18KVK39Vyavaharika Kannada (Kannada for communication) is for non-kannada speaking, reading and writing students and 18KAK39 Aadalitha Kannada (Kannada for Administration) is for students who speak, read and write kannada.

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

10	NC MC	18MATDIP31	Additional Mathematics - I	Mathematics	02	01	--	03	40	60	100	0

(a)The mandatory non – credit courses Additional Mathematics I and II prescribed for III and IV semesters respectively, to the lateral entry Diploma holders admitted to III semester of BE/B.Tech programs,shall attend the classes during therespective semesters to complete all the formalities of the course and appear for the University examination.In case, any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured F grade. In such a case, the students have to fulfill the requirements during subsequent semester/s to appear for SEE.
(b)These Courses shall not beconsidered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

Courses prescribed to lateral entry B. Sc degree holders admitted to III semester of Engineering programs

Lateral entrant students from B.Sc. Stream, shall clear the non-credit courses Engineering Graphics and Elements of Civil Engineering and Mechanics of the First Year Engineering Programme. These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

AICTE Activity Points to be earned by students admitted to BE/B.Tech/B.Plan day college programme (For more details refer to Chapter 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 years Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Point Programme. Students transferred from other Universities to fifth semester are required to earn 50 Activity Points from the year of entry to VTU. The Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the student from the year of entry to the programme. However, minimum hours' requirement should be fulfilled. Activity Points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

ACADEMIC CALENDER 2021-22

S J P N Trust's
Hirasugar Institute of Technology, Nidasoshi.
Inculcating Values, Promoting Prosperity
Approved by AICTE, Recognized by Govt. of Karnataka and Affiliated to VTU Belagavi.
Recognized Under Section 2(f) of UGC Act, 1956.
Accredited at ' A' Grade by NAAC, Programmes Accredited by NBA: CSE, ECE, EEE& ME.

IQAC
File I-11
2021-22 (Odd)
Rev: 00

CALENDAR OF EVENTS FOR THE ACADEMIC YEAR 2021-22 (ODD)

Date	Events
01-10-2021	Commencement of V/VII Semester Classes
02-10-2021	Gandhi Jayanthi & Swachh Bharat Abhiyan
18-10-2021	Commencement of III Semester Classes
01-11-2021	Kannad Rajyotsava
20-11-2021	Awareness Program on NEP
25-11-2021 to 27-11-2021	First Internal Assessment for III/V/VII Semester
29-11-2021	Feedback-I on Teaching-Learning
01-12-2021	Display of 1st Internal Assessment Marks and submission of Feedback-I to office
02-12-2021 to 04-12-2021	EDP Activities/ Green Club Activities
11-12-2021	Awareness Program on NEP
27-12-2021 to 29-12-2021	Second Internal Assessment for III/V/VII Semester
30-12-2021	Feedback-II on Teaching-Learning
03-01-2022	Display of 2nd Internal Assessment Marks and submission of Feedback-II to office
10-01-2022	Sports Day
11-01-2022	HSIT-Quest 2022
12-01-2022	HSIT-Fest 2022
13-01-2022	Blood Donation Camp
24-01-2022 to 25-01-2022	Lab Internal Assessment for V/VII Semester
27-01-2022 to 29-01-2022	Third Internal Assessment for V/VII Semester
31-01-2022	Display of Final Marks of V/VII Semester
31-01-2022	Last working day of V/VII Semester
10-02-2022 to 12-02-2022	Third Internal Assessment for III Semester
14-02-2022 to 15-02-2022	Lab Internal Assessment for III Semester
17-02-2022	Display of Final Marks of III Semester
19-02-2022	Last working day of III Semester
01-02-2022 to 10-02-2022	Practical Examinations for V/VII Semester
11-02-2022 to 25-03-2022	Theory Examinations for V/ VII Semester
21-02-2022 to 04-03-2022	Practical Examinations for III Semester
07-03-2022 to 25-03-2022	Theory Examinations for III Semester

October-2021

S	M	T	W	T	F	S
					1	2
3	4	5	6	7	8	9
10	11	12	13	14	15	16
17	18	19	20	21	22	23
24	25	26	27	28	29	30
31						

2-Gandhi Jayanthi, 6-Mahalaya Amavasya
14-Mahanavami, Ayudhapooja
15-Vijayadashami
20-Valmiki Jayanthi, Eid-Milad

November-2021

S	M	T	W	T	F	S
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30				

1-Kannada Rajyotsava, 3-Naraka Chaturdashi
5-Balipadyami Deepavalli
22-kanakadasa Jayanti

December-2021

S	M	T	W	T	F	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

25-Christmas

January-2022

S	M	T	W	T	F	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30	31					

14-Makar Sankranti, 26-Republic Day

February-2022

S	M	T	W	T	F	S
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28					

01/10/2021
Dr. B. V. Madiggond
IQAC Coordinator

01/10/21
Dr. S. C. Kamate
Principal

Subject Title	**TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES**		
Subject Code	18MAT31	**IA Marks**	40
Number of Lecture Hrs /	04	**Exam Marks**	60
Total Number of Lecture Hrs	50	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. S. S.Thabaj	Designation: Asst. Professor	Experience: 10
No. of times course taught: 03	**Specialization:** Mathematics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	II	Advanced Calculus & Numerical Methods

2.0 Course Objectives

Course Learning Objectives:

- To have an insight into Fourier series, Fourier transforms, Laplace transforms, Difference equations and Z- Transforms.
- To develop the proficiency in variational calculus and solving ODE's arising in engineering applications, using numerical methods.

3.0 Course Outcomes

On completion of this course, students are able to:

	Course Outcome	POs
CO1	Use Laplace transform and inverse Laplace transform in solving differential/ integral equation arising in network analysis, control systems and other fields of engineering.	1,2,3
CO2	Demonstrate Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing and field theory.	1,2,3
CO3	Make use of Fourier transform and Z-transform to illustrate discrete/continuous function arising in wave and heat propagation, signals and systems.	1,2,3
CO4	Solve first and second order ordinary differential equations arising in engineering problems using single step and multistep numerical methods.	1,2,3
CO5	Determine the externals of functional using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.	1,2,3
Total Hours of instruction		50

4.0 Course Content

MODULES	RBT Levels	No. Of Hours
MODULE-1 **Laplace Transform:** Definition and Laplace transforms of elementary functions (statements only). Laplace transforms of Periodic functions (statement only) and unit-step function – problems. **Inverse Laplace Transform**: Definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) and problems. Solution of linear differential equations using Laplace transforms.	**L1,L2**	**10**
MODULE-2 **Fourier Series**: Periodic functions, Dirichlet's condition. Fourier series of periodic functions period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.	**L1, L2**	**10**
MODULE-3 **Fourier Transforms:** Infinite Fourier transforms, Fourier sine and cosine transforms. Inverse Fourier transforms. Problems. **Difference Equations and Z-Transforms:** Difference equations, basic definition, z-transform-definition, Standard z-transforms, Damping and shifting rules, initial value and final value theorems (without proof) and problems, Inverse z-transform and applications to solve difference equations.	**L1, L2**	**10**
MODULE-4 **Numerical Solutions of Ordinary Differential Equations(ODE's)**: Numerical solution of ODE's of first order and first degree- Taylor's series method, Modified Euler's method. Runge -Kutta method of fourth order, Milne's and Adam-Bash forth predictor and corrector method (No derivations of formulae)-Problems.	**L1, L2**	**10**
MODULE-5 **Numerical Solution of Second Order ODE's:** Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). **Calculus of Variations:** Variation of function and functional, variational problems, Euler's equation, Geodesics, hanging chain, problems.	**L1,L2,L3**	**10**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	Common to all	Common to all engineering Subjects	Signal and Analysis, Field Theory, Thermodynamics, Fluid Dynamics etc

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Numerical methods are used to solve engineering problems. For examples will be drawn from a variety of engineering problems, including heat transfer, vibrations, dynamics, fluid mechanics, etc.
02	Special functions are used to wave propagation and scattering, fiber optics, heat conduction in solids, and vibration phenomena.
03	In sampling is the reduction of a to a. A common example is the conversion of a (a continuous signal) to a sequence of samples (a discrete-time signal).

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Calculus of Variations

8.0 Books Used and Recommended to Students

Text Books

17. 'B.S. Grewal, Higher Engineering Mathematics, 44th Edition 2017, Khanna Publishers.
18. E. Kreyszig: Advanced Engineering Mathematics, John Wiley & Sons, 10th Ed., 2016.
19. Srimanta Pal et al Engineering Mathematics, 3rd Edition, 2016, Oxford University Press.

Reference Books

1 N P Bali and Manish Goyal, "A text book of Engineering mathematics" , Laxmi publications, 6th Edition, 2014.
2. B.V.Ramana "Higher Engineering M athematics" Tata McGraw-Hill, 11th Edition, 2010 .
3. H. K Dass and Er. RajnishVerma ,"Higher Engineerig Mathematics", S. Chand Publishing, 1st Edition, 2011.
4. C. Ray Wylie,Louis C. Barrett "Advanced Engineering Mathematics" ,McGraw-Hill Book Co, 6th Edition, 1995
5. Chandrika Prasadand Reena Garg, "Advanced Engineering Mathematics", Khanna Publishing,2018

Additional Study material & e-Books

1. N.P.Bali & Manish.Goyal, a Text book of Engineering Mathematics, 7th edition, Laxmi Publications.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References

Web links and Video Lectures:
1. http://nptel.ac.in/courses.php?disciplineID=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://academicearth.org/
4. VTU EDUSAT PROGRAMME - 20

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	+ Plus Magazine	https://plus.maths.org/issue44.
2	Mathematics Magazine	www.mathematicsmagazine.com

11.0 Examination Note

Internal Assessment: 40 Marks

Theoretical aspects as well as relevant sketches should be drawn neatly.

Scheme of Evaluation for Internal Assessment (40 Marks)

(a) Internal Assessment test in the same pattern as that of the main examination (All the three Internal Tests marks considered): **30**Marks.

(b) Assignments: **10** Marks

SCHEME OF EXAMINATION:

Question paper pattern:

Note: -The SEE question paper will be set for 100 marks and the marks will be proportionately reduced to 60.

1. The question paper will have **ten** full questions carrying equal marks.
2. Each full question consisting of **20** marks.
3. There will be **two** full questions (with a **maximum** of **four** sub questions) from each module.
4. Each full question will have sub question covering all the topics under a module.
5. The students will have to answer **five** full questions, selecting **one** full question from each module.

12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
MODULE-1	1	Definition, transforms of elementary functions & Properties	20
	2	Problems	
	3	Periodic function	
	4	Unit step function & Problems	
	5	Inverse Laplace Transforms	
	6	Convolution theorem	
	7	Solution of linear differential equations using Laplace Transforms	
	8	Problems	
MODULE-2	9	Introduction, Periodic functions, Dirichlet's conditions	20
	10	Fourier series of periodic functions of period 2π & Problems	
	11	Fourier series of periodic functions of arbitrary period 2l & Problems	
	12	Fourier series of even & odd functions	
	13	Problems	
	14	Half range Fourier series & Problems	
	15	Practical harmonic analysis	
	16	Problems	
MODULE-3	17	Introduction, Infinite Fourier transform	20
	18	Fourier sine transforms & Problems	
	19	Fourier cosine transforms & Problems	
	20	Inverse Fourier transforms & Problems	
	21	z-transform-definition & Standard z-transforms	
	22	Initial value and final value theorems (without proof) and problems	
	23	Inverse z-transform & Problems	
	24	Applications of z-transforms to solve difference equations	
MODULE-4	25	Numerical solution of ordinary differential equations of first order & first degree	20
	26	Taylor's series method & Problems.	
	27	Modified Euler's method & Problems	
	28	Runge -Kutta method of fourth order & Problems	
	29	Milne's predictor and corrector method	
	30	Problems	
	31	Adams-Bashforth predictor and corrector method	
	32	Problems.	
MODULE-5	33	Numerical solution of second order ordinary differential equations	20
	34	Runge -Kutta method & Problems.	
	35	Milne's method & Problems.	
	36	Problems.	
	37	Calculus of Variations: Variation of function and Functional, variation problems	
	38	Euler's equation	
	39	Problems	
	40	Geodesics & Hanging chain, problems	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity.	Book 1, of the reference list. Website of the Reference list
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
4	Assignment 4: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	10	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 QUESTION BANK

Module-1: Laplace & Inverse Laplace Transform;

1. Find the Laplace Transform of sin2t sin3t. & $\sin^3 2t$.
2. Find L (e^{3t}sin2t) & L (e^{4t} sin2tcost).
3. Find L[1-e^t]/t & L[cosat-cosbt/t]
4. Using unit step function find LT of $f(t) = \begin{cases} \sin t, & 0 < t < \pi \\ \sin 2t, & \pi < t < 2\pi \\ \sin 3t, & t > 2\pi \end{cases}$
5. Express $f(t) = \begin{cases} \cos t, & 0 < t < \pi \\ \cos 2t, & \pi < t < 2\pi \\ \cos 3t, & t > 2\pi \end{cases}$ in terms unit step function & hence find LT
6. Evaluate L[t^2u(t-3)].
7. Find the inverse transform s+2/s^2-4s+13.
8. Find L^{-1}[4s+5/$(s-1)^2(x+2)$]
9. Find L^{-1}[s/s^4+4a^4].
10. Find L^{-1}[s/$(s^2+a^2)^2$].
11. Find L^{-1}[log(s+1/s-1)]
12. Find L^{-1}[(s/(2s-1)(3s-1)].
13. Using the Convolution THM obtain the L^{-1}[s/$(s^2+a^2)2$] .
14. Solve the differential equation d^2y/dx^2-3dy/dx+2y = e^{3t} with y(0)=0=y'(0), using LT
15. Solve the differential equation y''+4y'+3y=e^{-t}, y(0) =1= y'(0). Using LT

Module-2: Fourier series:

1. Obtain a Fourier series to represent e^{-ax} from $(-\pi, x)$
2. Expand f(x) = x sin x, 0 < x < 2, in a Fourier series.
3. For a function f(x) defined by f(x) = |x |, $-\pi < x < \pi$, obtain a Fourier series. Deduce that $\frac{1}{1^2}+\frac{1}{3^2}+\frac{1}{5^2}+\frac{1}{7^2}=\frac{\pi^2}{8}$
4. Find the Fourier series for the function $f(x)=\frac{\pi-x}{2}$ in (0, 2π). Hence deduce that $\frac{\pi}{4}=1-\frac{1}{3}+\frac{1}{5}---$
5. Find the Fourier series to represent f(x) = x+x^2 from x=- π to x= π and deduce that $\frac{1}{1^2}-\frac{1}{2^2}+\frac{1}{3^2}-\frac{1}{4^2}=\frac{\pi^2}{12}$
6. Expand f(x) = e^{-x} as a Fourier series in the interval (–l, l)
7. Obtain Fourier series for the function
   $f(x)=\begin{cases}\pi x, & 0 \le x \le 1\\ \pi(2-x), & 1 \le x \le 2\end{cases}$ and deduce that $\frac{1}{1^2}+\frac{1}{3^2}+\frac{1}{5^2}+\frac{1}{7^2}$-------
8. Develop f(x) in Fourier series in the interval (-2, 2) if $f(x)=\begin{cases}0, & -2 < x < 0\\ 1, & 0 < x < 2\end{cases}$
9. Find the half range cosine series for the function f(x) = x^2 in the range 0 ≤ x ≤ 1
10. Find the complex form of the Fourier series of the periodic function f(x) = cos ax, in $-\pi < x < \pi$.
11. The following table gives the variation of periodic current over a period

t sec	0	T/6	T/3	T/2	2T/3	5T/6	T
A amp	1.98	1.30	1.05	1.30	-0.88	-0.25	1.98

Show that there is a direct current part of 0.75 amp in the variable current and obtain the amplitude of the first harmonic.

12. Obtain the Fourier series for the function f(x) = Hence deduce that $\frac{\pi^2}{8}=\frac{1}{1^2}+\frac{1}{3^2}+\frac{1}{5}+$

_____

13. Obtain the Fourier expansion of $f(x)=2x-x^2$ *in* $0 \le x \le 2$

14. Obtain the constant term and the coefficient of the first sine and cosine terms in the Fourier expansion of y as given below.

x	0	1	2	3	4	5
y	9	18	24	28	26	20

Module-3: Fourier Transforms*:*

1. Find the Fourier transform of
   $f(x)=\begin{cases}1, & |x|<1\\ 0, & |x|<1\end{cases}$ Hence evaluate $\int_0^\infty \frac{sinx}{x}dx$
2. Find the Fourier transform of the function
   $f(x)=\begin{cases}x, & |x| \le \\ 0, & |x|>\alpha\end{cases}$ Where α is a positive constant?
3. Find the Fourier transform of cosax^2
4. Find the Fourier sine transform of $e^{-ax/x}$
5. Find the Fourier sine and cosine transform of $f(x)=\begin{cases}1, & 0 \le x < a\\ 0, & x \ge a\end{cases}$
6. Find the finite Fourier sine and cosine transform of f(x) = 2x, 0 < x < 4.
7. Find the cosine transform of $f(x)=\frac{1}{1+x^2}$
8. Find the Fourier sine transform of $e^{-|x|}$
9. Find the Fourier transform of $f(x)=\begin{cases}a^2-x^2, & |x|<a\\ 0, & |x|>a\end{cases}$ and Evaluate $\int_0^\infty \frac{sinx-xcosx}{x^3}dx$.
10. Find the Fourier sine transform of $f(x)=\frac{e^{-ax}}{x}$, $a>0$.
11. Find the Fourier cosine transform of $(x)=\begin{cases}x, & 0<x<1\\ 2-x, & 1<x<2\\ 0, & x>2\end{cases}$.

12. Find the Fourier transform of $f(x) = e^{-|x|}$ and Evaluate $\int_0^\infty \frac{xsinmx}{1+x^2} dx$.
13. Find the Fourier transform of $f(x) = e^{-|x|}$ and Evaluate $\int_0^\infty \frac{xsinmx}{1+x^2} dx$.

Z- Transformation:

1. P.T. $z_T(n^2) = \frac{z^2+z}{(z-1)^3}$
2. P.T. $z_T(n^3) = \frac{z^3+4z^2+2}{(z-1)^4}$
3. P.T. $z_T(cos\theta) = \frac{z(z-cos\theta)}{z^2-2zcos\theta+1}$
4. P.T. $z_T(sin\theta) = \frac{(zsin\theta)}{z^2-2zcos\theta+1}$
5. P.T. $z_T(a^n cosn\theta) = \frac{z(z-acos\theta)}{z^2-2azcos\theta+a^2}$
6. Find the Z-transform of $cos\ hn\theta$ & $sinhn\theta$.
7. Find the Z-transform of $(n+1)^2$
8. Using the inversion integral method find the inverse Z-transform of $\frac{3z}{(z-1)(z-2)}$
9. Solve $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ $y_{n+2} + 6y_{n+1} + 9y_n = 2^n$ with $y_0 = y_n = 0$ using Z-transform
10. Solve the difference equation $y_{n+2} + 2y_{n+1} + y_n = n$ with $y_0 = y_n = 0$ using Z-Transform.
11. Obtain the z-transform of $cos\ n\theta$ and $sin\ n\theta$
12. Find the Inverse z-transform of $\frac{2z^2+3z}{(z+2)(z-4)}$.
13. If $\bar{u}(z) = \frac{2z^2+3z+12}{(z-1)^4}$, find the value of $u_0,\ u_1,\ u_2,\ u_3$.
14. Solve the difference equation $u_{n+2} + 6u_{n+1} + 9u_n = 2^n$, $u_0 = u_1 = 0$.

MODULE-4: Numerical Methods

1. Solve $\frac{dy}{dx} = x^2y - 1$with y(0)=1 using Taylor's series method and find y(0.1) consider upto 4th degree terms.
2. Use Runge Kutta fourth order method to solve $\frac{dy}{dx} = \frac{y^2-x^2}{y^2+x^2}$ with y(0)=1 and find y for x= 0.2 and 0.4 take h=0.2
3. Given $\frac{dy}{dx} = xy + y^2$, y(0)=1, y(0.1) =1.1169 ,y(0.2)=1.2773, y(0.3)=1.5049 find y(0.4) accurate upto three decimal places using Milne's predictour corrector method.
4. Applying R-K method to find an approximate value of y for x=0.2 in steps of 0.1 of $\frac{dy}{dx} = x + y^2$ given that y=1 when x=0.
5. Given $\frac{dy}{dx} = x^2(1 + y)$ & y(1)=1,y(1.1)=1.233, y(1.2) = 1.548,y(1.3) = 1.979. Evaluate y(1.4) by Adams Bash Fourth method
6. Employ Taylor's series method to find an approximate solution correct to fourth decimal places for the following initial value problem at x=0.1 & 0.2 $\frac{dy}{dx} = 2y + 3e^x$, y(0) = 0.
7. Using Milne's predictour corrector method find y where x=0.8 given $\frac{dy}{dx} = x - y^2$, y(0)=0, y(0.2)=0.02, y(0.4)=0.0795, y(0.6)=0.1762.Applying corrector formula twice.
8. Employ R-K method of 4rth order to solve the equation $\frac{dy}{dx} = 3x + y/2$, y(0)=1 at x=0.2 taking step length h=0.1
9. Solve the differential equation $\frac{dy}{dx} = x^2 + y^2$ given y(0)=1 to find the value of y(0.1) by using Taylor's series method of order.
10. Using modified Euler's method ,solve the equation $\frac{dy}{dx} = \frac{1}{x+y}$, y(0)=1 in steps of 0.5 at x = 1
11. Using Adams Bash fourth predictor correct method find y when x=0.8 given $\frac{dy}{dx} = x - y^2$, y(0)=0, y(0.2)=0.02, y(0.4)=0.0795, y(0.6)=0.1762. Apply correct formula twice.

12. Using Taylor's series method to find y at the point x=0.1& x=0.2 given that $\frac{dy}{dx} = x^2 + y^2$,y(0)=1
13. From the data given below find y at x=1.4 using Milne's predictour corrector method y'= x^2+y/2

x	1	1.1	1.2	1.3
y	2	2.2156	2.4649	2.7514

MODULE-5: **Numerical Methods And Calculus Of Variation**

1. Use R- K method to solve $y = xy'^2 - y^2$ for x = 0.2 correct to 4 decimal places. $y(0) = 1$ & $y'(0) = 0$
2. Evaluate $y(0.2)$ by RK method given that $y'' - x(y')^2 + y^2 = 0, y(0) = 1, y'(0) = 0$
3. Given $y'' - xy' - y = 0$ with the initial conditions y(0)=1, y'(0)=0. Compute y(0.2) and y'(0.2) by taking h=0.2 and using fourth order Runge Kutta method.
4. Obtain the solution of the equation $2\frac{d^2y}{dx^2} = 4x + \frac{dy}{dx}$ at the point x = 1.4 by applying Milne's method given that y(1) = 2, y(1.1) = 2.2156, y(1.2) = 2.4649. y(1.3) = 2.7514, y' (1) = 2, y'(1.1) = 2.3178, y'(1.2) = 2.6725 and y'(1.3) = 3.0657.
5. Using R-K method of order four, solve y" = y+xy', y(0) = 1 , y'(0) to find y(0.2) & y'(0.2).
6. Show that the Geodesics on a plane are straight line.
7. Find the Geodesics on a right circular cylinder of radius a.
8. Find the extremals of the functional $\int_{x_0}^{x_1} \frac{(y')^2}{x^3} dx$
9. Show that the shortest distance between any two points in a plane is a straight line.
10. Prove that Catenary is the curve which when rotated about a line generates a surface of minimum area.
11. Find the extremal of the functional $\int_0^{\pi} (y'^2 - y^2 + 4y\cos x) dx;\ y(0) = 0 = y(\pi)$
12. Solve the variational problem $\delta \int_1^2 (x^2(y')^2 + 2y(x+y)) dx = 0$, given $y(1) = y(2) = 0$
13. Find the path on which a particle in the absence of friction will slide from one point to another in a shortest time under the action of gravity.
14. Find the curve passing through the point (x_1, y_1) and (x_2, y_2) which when rotated about the x axis gives the minimum surface area.
15. Find the curve on which the functional $\int_0^1 (y'^2 + 12xy)\, dx$ with $y(0) = 0$ and $y(1) = 1$ can be extremised.

16.0 University Result

Examination	FCD (S+, S, A)	FC (B)	SC (C, D, E)	% Passing
Jan 2020-21	13	9	2	80

Prepared by	Checked by		
Prof. S. S. Thabaj	Prof. S. L. Patil	**HOD**	**Principal**

Subject Title	**NETWORK THEORY**		
Subject Code	18EC32	**CIE Marks**	40
Number of Lecture Hrs / Week	03 + 2(Tutorials)	**Semester End Exam Marks**	60
Total Number of Lecture Hrs	50	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof. P.V.Patil	**Designation:** Asst Professor	**Experience:**09yrs 02 Months.
No. of times course taught: 06	**Specialization:** VLSI Design & Embedded Systems.	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I	Engineering Mathematics I
02	ECE	II	Engineering Mathematics II
03	EEE	I/II	Basic Electrical

2.0 Course Objectives

This course will enable students to:

- Describe basic network concepts emphasizing source transformation, source shifting, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power.
- Explain network Thevenin‘s, Millman‘s, Superposition, Maximum Power transfer and Norton‘s Theorems and apply them in solving the problems related to Electrical Circuits.
- Explain the behavior of networks subjected to transient conditions.
- Use applications of Laplace transforms to network problems.
- Study two port network parameters like Z, Y, T and h and their inter-relationships and applications.
- Study of RLC Series and parallel tuned circuit.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	RBT Level	POs
C202.1	Determine currents and voltages using source transformation/source shifting/mesh/nodal analysis and reduce given network using star delta transformation/source transformation / source shifting.	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12
C202.2	Solve network problems by applying superposition/Reciprocity/Thevenin’s Norton’s/Maximum power transfer/Milliman’s network theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.	L1 , L2, L3, L4	PO1, PO2, PO3, PO4, PO12
C202.3	Calculate current and voltage for the given circuit under transient conditions.	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12
C202.4	Apply Laplace transform to solve the given network.	L1 , L2, L3,	PO1, PO2, PO3, PO4, PO12
C202.5	Evaluate for RLC elements/frequency response related parameters like resonant frequency, quality factor ,half power frequencies, voltage across inductor and capacitor, current through RLC elements in resonant circuits.	L1 , L2, L3, L4	PO1, PO2, PO3, PO4, PO12

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks.	**10 Hours**	**L1 , L2, L3, L4**
Module 2: Network Theorems: Superposition, Millman's theorems, Thevinin's and Norton's theorems, Maximum Power transfer theorem.	**10 Hours**	**L1 ,L2,L3 ,L4**
Module 3: Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.	**10 Hours**	**L1 ,L2,L3**
Module 4: Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.	**10 Hours**	**L1 ,L2,L3 ,L4**
Module 5: **Two port network parameters:** Definition of Z, Y, h and Transmission parameters, modeling with these parameters, relationship between parameters sets. **Resonance: Series Resonance:** Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance. **Parallel Resonance:** Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.	**10 Hours**	**L1 ,L2,L3 ,L4**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	V	Analog Communication	Network analysis concepts
02	VI	CMOS VLSI design	Network analysis concepts

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Analyze different types of Network
02	Design of different types of Networks

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Network Analysis
02	NPTEL	Application

8.0 Books Used and Recommended to Students

Text Books
1. M.E. Van Valkenberg (2000), "Network analysis", Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958. 2. 2. Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006, ISBN: 9788122427677.
Reference Books
1. Hayt, Kemmerly and Durbin "Engineering Circuit Analysis", TMH 7th Edition, 2010. 2. J.David Irwin/R.Mark Nelms,",Basic Engineering Circuit Analysis",John Wiley,8 th ed,2006 3. Charles K Alexander and Mathew N O Sadiku,"Fundamentals of Electric circuits",Tata McGraw-Hill,3 rd edition,2009
Additional Study material & e-Books
1. J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", John Wiley, 8th edition, 2006 2. VTU on line notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
01) https://nptel.co.in 02) http://m.noteboy.in/vtuflies/machine%20drawing.pdf

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	Website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of three will be accounted.

Scheme of Evaluation for Internal Assessment (40 Marks)
30 marks for IA Test & 10 marks for Assignment.

SCHEME OF EXAMINATION:
Two main questions to be set from the syllabus covered.
Question 1 or 2
Answer both main questions.
Question 1 = 15 marks.
Question 2 = 15 marks.
Total = 30 marks

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Practical sources	20
	2	Source transformations	
	3	Network reduction using Star – Delta transformation	
	4	Loop analysis With linearly dependent and independent sources for DC Networks.	
	5	Loop analysis With linearly dependent and independent sources for DC Networks.	
	6	Loop analysis With linearly dependent and independent sources for AC Networks.	
	7	Loop analysis With linearly dependent and independent sources for AC Networks.	
	8	Node analysis With linearly dependent and independent sources for DC networks	
	9	Node analysis With linearly dependent and independent sources for AC networks	
	10	Problems	
2	1	Superposition theorem,	40
	2	Problems on Superposition Theory	
	3	Thevenins theorem	
	4	Problems on Thevenins theorem	
	5	Nortons Theorem	
	6	Problems on Nortons Theorem	
	7	Millimans Theorem	
	8	Problems on Millimans Theorem.	
	9	Maximum power transfer Theorem	
	10	Problems on Maximum power transfer Theorem	
3	1	Behavior of circuit elements under switching conditions and their representation	60
	2	Behavior of circuit elements under switching conditions and their representation	
	3	Behavior of circuit elements under switching conditions and their representation	
	4	Behavior of circuit elements under switching conditions and their representation	
	5	Evaluation of initial and final conditions in RL circuits for DC excitations	
	6	Evaluation of initial and final conditions in RC circuits for DC excitations	
	7	Evaluation of initial and final conditions in RLC circuits for DC excitations	
	8	Evaluation of initial and final conditions in RL circuits for AC excitations	
	9	Evaluation of initial and final conditions in RC circuits for AC excitations	
	10	Evaluation of initial and final conditions in RLC circuits for AC excitations	
4	1	Solution of networks, Step response	80
	2	Solution of networks, Step response	
	3	Solution of networks, Ramp response	
	4	Solution of networks, Ramp response	
	5	Solution of networks, Impulse response	
	6	Solution of networks, Impulse response	

	7	Waveform Synthesis.	
	8	Waveform Synthesis.	
	9	Waveform Synthesis.	
	10	Waveform Synthesis.	
5	1	Definition of z, y, h parameters	100
	2	Definition of transmission parameters	
	3	Modeling with these parameters	
	4	Relationship between parameter sets.	
	5	Series Resonance: Variation of Current and Voltage with Frequency.	
	6	Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor	
	7	Selectivity with Variable Capacitance, Selectivity with Variable Inductance	
	8	Parallel Resonance: Selectivity and Bandwidth	
	9	Maximum Impedance Conditions with C, L and f Variable current in Anti-	
	10	The General Case-Resistance Present in both Branches	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

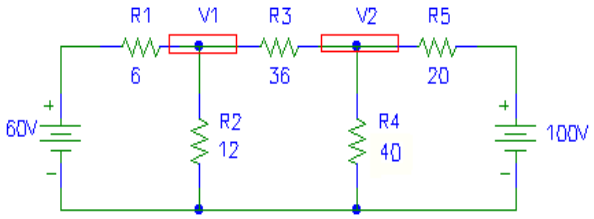
Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Basic Concepts	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
2	Assignment 2: University Questions on Network theorems	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2, of the syllabus	4	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions on Transient Behavior & Initial Conditions, Laplace transformation and application	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
4	Assignment 4: University Questions Resonant Circuits and Two port network parameters.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions Resonant Circuits and Two port network parameters.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	12	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list

14.0 QUESTION BANK

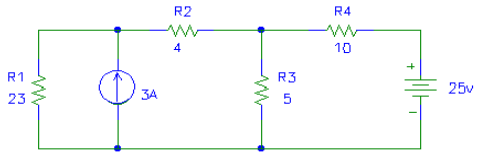
MODULE -1

1. State Ohm's law and its limitations.
2. Name different network elements.
3. What is meant by Electric Circuits?
4. State two salient points of a series combination of resistance.
5. State two salient points of a parallel combination of resistance
6. Give two applications of both series and parallel combination.

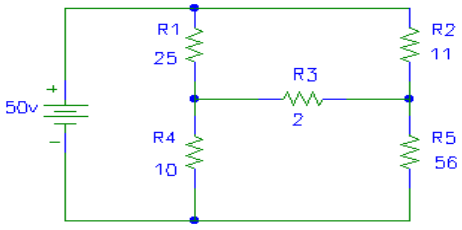
7. State Kirchhoff's law.
8. Give two applications of both series and parallel combination.
9. Find the equivalent current source for a voltage source of 100 V with series resistance of 2 ohm.
10. Write the expression for converting delta connected resistances into an equivalent star connected resistances.
11. A Y-connected resistive network consists of 2 ohm in each arm. Draw the equivalent delta-connected network and Define the dependent source of a circuit.
12. Write the voltage division and current division rule.
13. What is meant by Mesh Analysis?
14. What is meant by Nodal analysis?
15. Define an ideal voltage source.
16. Define an ideal current source
17. Draw the symbolic representation of the voltage source and current source.
18. Explain how voltage source with a source resistance can be converted into an equivalent current source.
19. Explain how current source with a parallel resistance can be converted into an equivalent voltage source.
20. Define the dependent source of a circuit.
21. Define the current division rule
22. A bulb is as rated 230V, 230W. Find the rated current, resistance of the filament and the energy consumed when it is operated for 10 hours.
23. Draw the V-I relationship of an ideal voltage source
24. Find the node voltages V1 and V2.



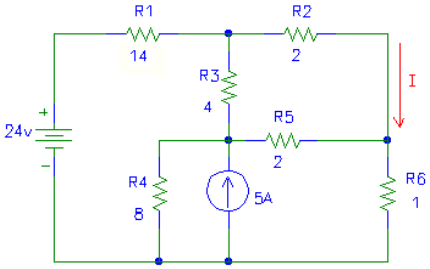
25. Find the current through R2 and R3 using mesh analysis.



26. Find the voltage across R3 using Nodal analysis.

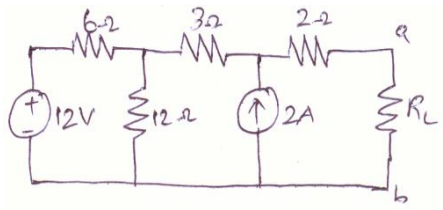


27. Find the current labeled "I" using both mesh and node analysis.

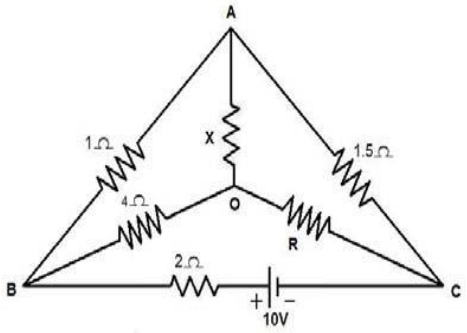


MODULE -2

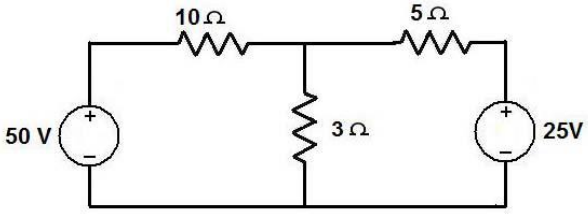
1. State Superposition theorem.
2. State and Explain Thevenin's Theorem.
3. State and explain Norton's theorem.
4. State Maximum Power Transfer Theorem.
5. Determine Thevenin's equivalent across the terminals AB for the circuit shown in figure below.
6. State reciprocity theorem.
7. Write some applications of Maximum power transfer theorem.
8. The power delivered is maximum, if the load impedance is equal to the supply circuit impedance – True or False.
9. What is the condition for maximum power transfer?
10. Find the value of RL for maxim um power transfer in the circuit of figure. Find the maximum power



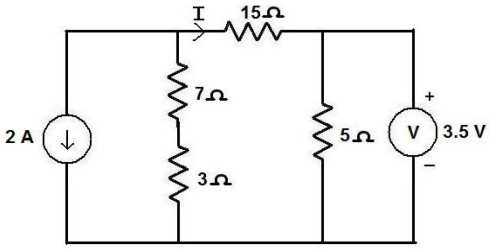
11. (i) Find the value of R and the current flowing through it in the circuit shown when the current in the branch OA is zero.



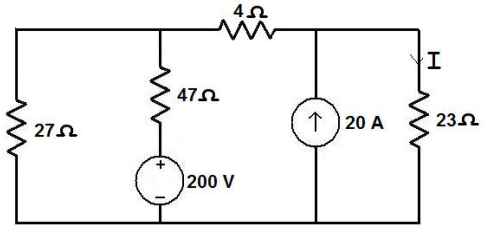
12. Find the current in each resistor using superposition principle of figure.



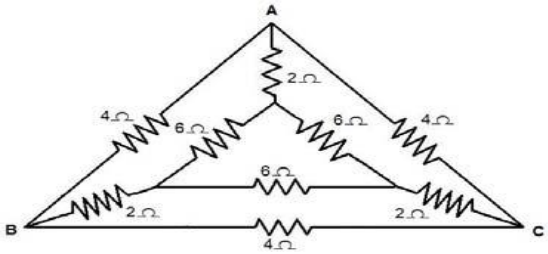
13. For the circuit shown, use superposition theorem to compute current I.



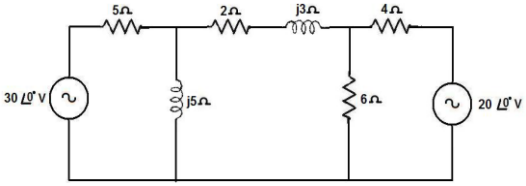
14. (i)Compute the current in 23 ohm resistor using super position theorem for the circuit shown below.



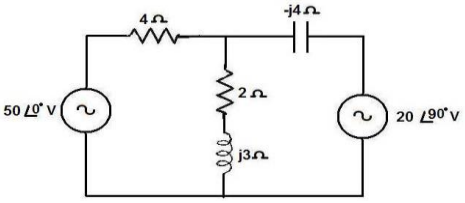
(ii) Find the equivalent resistance between B and C in figure



15. Using superposition theorem calculate current through (2+j3) ohm impedance branch of the circuit shown.



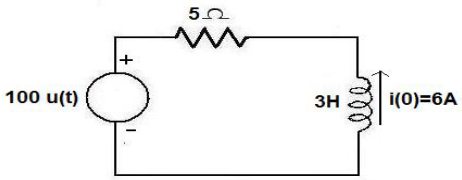
16. For the circuit shown, determine the current in (2+j3) ohm by using superposition theorem.



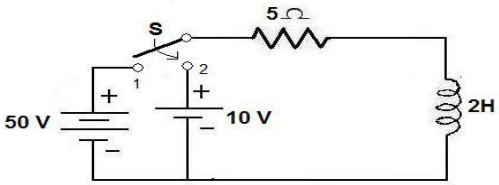
MODULE -3

1. The transients are due to the presence of energy storing elements in the circuit –True or false.
2. What is a step function?
3. What is an initial condition?
4. What is a transient?
5. What is the steady state value?
6. Write the transient current equation when RL series circuit is connected to a step voltage of volts.
7. A DC voltage of 100 volts is applied to a series RL circuits with R = 25 ohm what will be the current in the circuit in the circuits at twice the time constant?
8. Sketch the current given by I (t) = 5 – 4 e-20 t.
9. Distinguish between free and forced response.
10. Draw the equivalent circuit for inductor and capacitor at t = 0+ when there is no initial energy.
11. Define a time constant of a RL circuit.
12. Draw the equivalent circuits for the inductor and capacitor at t=0+ with presence of initial energy.
13. Distinguish between the steady state and the transient response of an electrical circuit.
14. Define a time constant of a RC circuit.
15. Draw the equivalent circuit at t = 0+ for a capacitor with initial charge of q 0.
16. Sketch the response of RC network for a unit step input.
17. What are the periodic inputs?
18. What are critical frequencies? Why are they so called?
19. Draw the transient response of R-L circuits for step input.

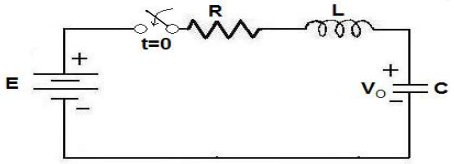
20. Define the time constant of a transient response.
21. Find the time constant of RL circuits having R = 10 ohm and L = 0.1 mH.
22. What is meant by critical damping?
23. In the circuit of the figure shown below, find the expression for the transient current and the initial rate of growth of the transient current .



24. In the circuit shown in figure, switch S is in position 1 for a long time and brought to position 2 at time t=0. Determine the circuit current.



25. A resistance R and 2 microfarad capacitor are connected in series across a 200V direct supply. Across the capacitor is a neon lamp that strikes at 120V. Calculate R to make the lamp strike 5 sec after the switch has been closed. If R = 5Megohm,how long will it take the lamp to strike?
26. A Series RLC circuits has R=50 ohm, L= 0.2H, and C = 50 microfarad. Constant voltage of 100V is impressed upon the circuit at t=0. Find the expression for the transient current assuming initially relaxed conditions.
27. A Series RLC circuits with R=300 ohm, L=1H and C=100x10-6 F has a constant voltage of 50V applied to it at t= 0. Find the maximum value of current (Assume zero initial conditions)
28. A step voltage V(t) = 100 u(t) is applied to a series RLC circuit with L=10H, R=2ohm and C= 5F. The initial current in the circuit is zero but there is an initial voltage of 50V on the capacitor in a direction which opposes the applied source. Find the expression for the current in the circuit.



29. In the circuit shown in Fig.6.56, the switch is thrown from position 1 to 2 at t = 0.Just before the switch is thrown, the initial conditions are i(O-) =2A and vc(O-) =2V. Find i(t) after the switching action, using Laplace transform method.

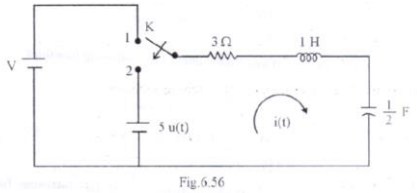


Fig.6.56

30. In the circuit shown in Fig.6.57, the switch. is closed at t. = 0, with zero initial conditions. Find i(t) using L.T. method.

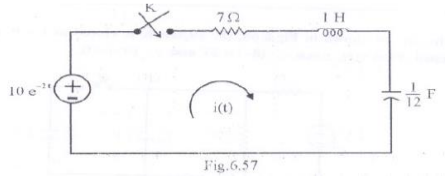


Fig.6.57

31. In the circuit shown in Fig.6.58, find i_2 (t) after the switch is closed at t = 0, using transformed circuit.

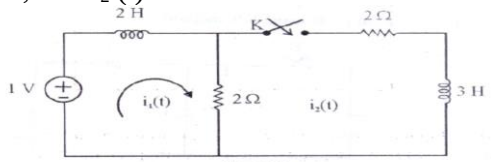


Fig.6.58

32. In the circuit shown in 6.59,the switch is closed at t=0, find $V_L(t)$ using transformed circuit.

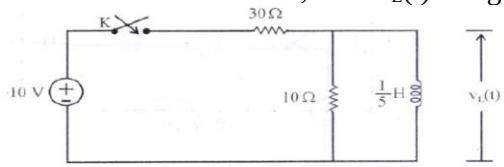


Fig.6.59

33. In the circuit shown in Fig.6.60, the switch K is closed at t = 0, after steady state is reached. Find v(t), given $V_{C1}(0-) = 2V$ and $v_{C2}(0-) = 0$ v .

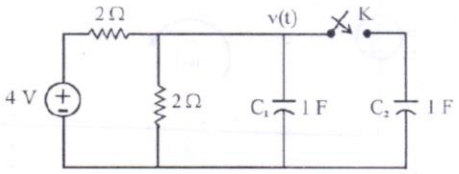


Fig.6.60

34. At t = 0, the switch K is opened in the network shown in Fig.6.61. Find the value of V1 (t) and V2 (t) for all t > 0, using L.T method.

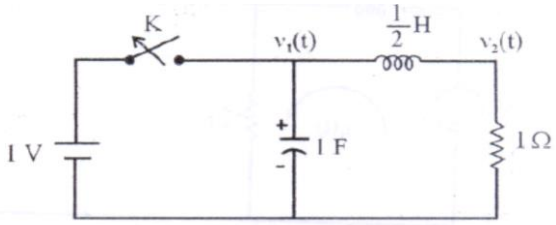


Fig.6.61

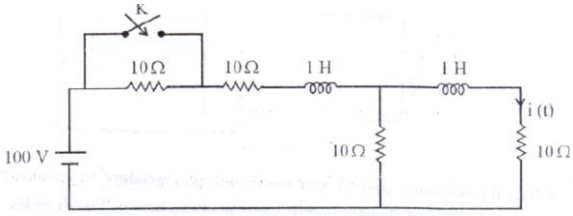


Fig.6.64

MODULE -4

1. A pulse voltage of width 'a' and magnitude 20 V is applied at t = 0, to an R-L series circuit consisting of R =5Ω and L =3H. Find i (t) using L.T method. Assume zero initial conditions.
2. A voltage pulse of width 'a' and magnitude 10 V is applied at t =0 to an R-C series circuit consisting of R =1 Ω and C =1/5F. Find i(t). Assume zero charge on C, before the application of the voltage pulse.
3. Find the response current of a series R-L circuit consisting of R =4 Ω and L =2 H, when each of the Following driving force voltages are applied.
4. i) Unit ramp voltage r *(t* - 5) ii) Unit impulse voltage δ *(t* - 5) iii) Unit step voltage u (t) - Assume zero initial conditions.
5. Find the current i(t) in a series R-C circuit consisting of R =4 Ω and C =1/5 F, when each of the following voltages are applied. Assume zero initial conditions.
6. i) r *(t* - 2) ii) u *(t* - 2) iii)δ *(t* - 2)

7. Find the impulse response in the circuit shown in Fig.6.65, if the output is V_L (t).

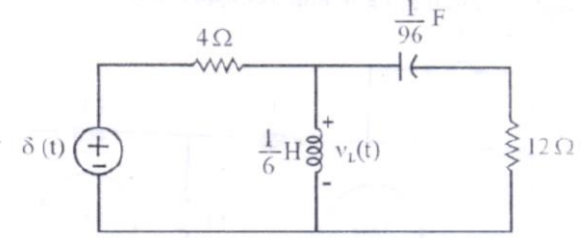


Fig.6.65

8. The network shown in Fig.6.66 is initially in relaxed state. When the source is 10 u (t) volts, the transform of the input current is 10 / (2s + 4). The circuit is brought to its initial state once again. Find the impedance and input response Vs(t), when the source is a current generator of 5 e^{-2t} amperes.

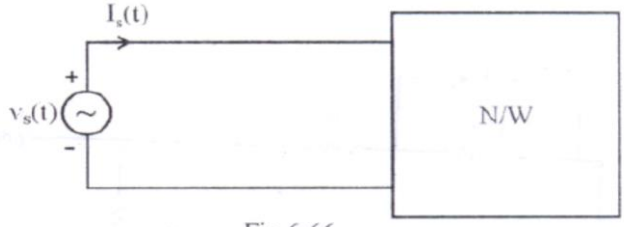


Fig.6.66

9. Given the following sources and the results they produce in a single element circuit. Deduce the type of element and its value in-ohms, henrys, farads as the case may be. If the source is a voltage, the response is current and vice versa.

	Source	Response
i)	i (t) = 5 δ(t)	10 u(t)
ii)	i (t) = 5 u(t)	3 δ(t)
iii)	e (t) = 10 u(t)	5 δ(t)
iv)	i (t) = 3/2 δ(t)	9/4 δ(t)
v)	e(t) = 1/3 δ(t)	3 u(t)

10. The periodic current waveform is as shown in Fig.6.67. Find its Laplace transform equation.

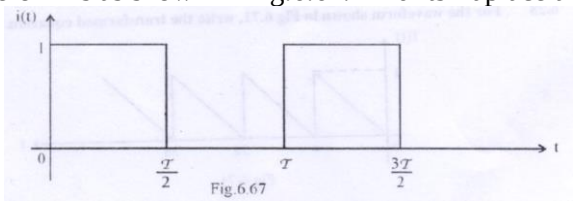


Fig.6.67

11. Find the Laplace transform of the following functions.
    i) $10\,t^3 - 5\cos 3t + 8\sin t$ ii) $e^{-3t}\sin^3 3t$ iii) $t\cos(wt+\theta)$
    iv) $e^{3t}\cos^3 2t$ v) $t^2 e^{-at}\cos wt$

12. Find the inverse Laplace transforms of the following questions:

i) $\dfrac{2s+6}{s^2+6s+5}$ ii) $\dfrac{2s}{(s^2+4)(s^2+5)}$ iii) $\dfrac{s+5}{s^2+2s+5}$

iv) $\dfrac{1}{(s+1)(s+1)^2}$ v) $\dfrac{s^3-s^2-3s+9}{(s+2)(s^2+4)}$ vi) $\dfrac{s+2}{s^2-4s+12}$

vii) $\dfrac{2s^2-6s+5}{s^3-6s^2+11s-6}$ viii) $\dfrac{s^3-s^2-3s+9}{s^2(s^2+9)}$

13. Solve the following differential equations using Laplace transform method.

i) $\frac{d^2i}{dt^2} + 4\frac{di}{dt} + 8i = 8\,u(t)$, given $i(0+) = 3$ and $\frac{di}{dt}(0+) = -4$

ii) $\frac{d^2x}{dt^2} - 2\frac{dx}{dt} + x = e^t$, given $x(0+) = 2$ and $x^1(0+) = -1$

iii) $\frac{d^2i}{dt^2} + 2\frac{di}{dt} + 4i = -4\sin 2t$, given $i(0+) = 1$ and $i(0+) = -1$

iv) $\frac{d^2i}{dt^2} + 4\frac{di}{dt} + 3i = -12\,e^{-3t}$, given $i(0+) = 0$ and $i^1(0+) = 4$

v) $2\frac{d^3i}{dt^3} + 9\frac{d^2i}{dt^2} + 13\frac{di}{dt} + 6i = 0$, given $i(0+) = 0$, $i^1(0+) = 1$ and $i^{11}(0+) = -1$

14. Find the initial and final values of the following functions:

i) $\frac{1}{s(s^2 - a^2)}$ ii) $\frac{s^3 + 7s^2 + 5}{s(s^3 + 3s^2 + 4s + s)}$ iii) $\frac{2s+3}{(s+1)(s+3)}$ iv) $\frac{e^{-2s}(s+2)}{s^3 + 5s}$

v) $\frac{2(s+1)(s+3)}{(s+2)(s+6)}$ vi) $\frac{(s+1)\sin\theta + b\cos\theta}{(s+a)^2 + b^2}$ vii) $\frac{8(s^2 + 2s + 1)}{(s+2)(s^2+4)}$

15. Find the inverse Laplace transform of the following functions, using convolution theorem.

i) $\frac{s}{(s^2 - a^2)^2}$ ii) $\frac{s}{(s^2+a)(s^2+25)}$ iii) $\frac{1}{s(s^2 - a^2)}$ iv) $\frac{s+1}{s(s^2+4)}$ v) $\frac{5}{s^2(s+2)^2}$

16. Using convolution theorem, find v(t), in the circuit shown in Fig.6.54.

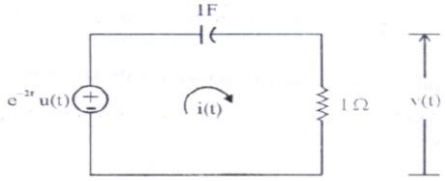
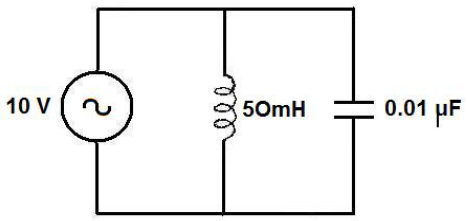


Fig. 6.54

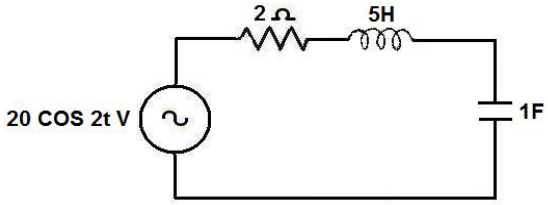
MODULE -5

A. RESONANCE

1. Define Q-factor of a coil.
2. Define bandwidth of a resonant circuit.
3. Find the resonant frequency in the ideal parallel LC circuit shown below

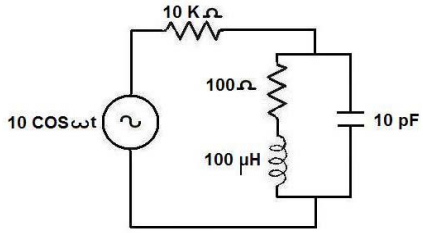


4. Find the impedance offered to the source by the load.



5. State the condition for resonance in RLC series circuit.
6. A resistance 5 ohms, inductance 0.02H and capacitor 5 microfarads are connected in series. Find the resonance frequency and the power factor at resonance.
7. Two capacitances C1 and C2 of values 10µF and 5µF are connected in series. What is the equivalent capacitance of this combination?
8. Derive bandwidth for a series RLC circuit as a function of resonant frequency.

9. (i) For the circuit below, find the value of ω so that current and source emf are in phase. Also find the current at this frequency.



(ii) Discuss the characteristics of parallel resonance of a circuit having G,L and C.

10. (i) A Pure resistor, a pure capacitor and a pure inductor are connected in parallel across a 50Hz supply, find the impedance of the circuit as seen by the supply. Also find the resonant frequency.
(ii) When connected to a 230V, 50Hz single phase supply, a coil takes 10kVA and 8kVAR. For this coil calculate resistance, inductance of coil and power consumed.
11. (i) In an RLC series circuit if ω1 and ω2 are two frequencies at which the magnitude of the current is the same and if ωr is the resonant frequency, prove that $\omega r^2 = \omega 1 \omega 2$.
(ii) A series RLC circuit has Q = 75 and a pass band (between half power frequencies) of 160 Hz. Calculate the resonant frequency and the upper and lower frequencies of the pass band.
12. (i) Explain and derive the relationships for bandwidth and half power frequencies of RLC series circuit.
(ii) Determine the quality facto of a coil R = 10 ohm, L = 0.1H and C = 10 μf
13. A series RLC circuit has R=20 ohm, L=0.005H and C = 0.2 x 10-6 F. It is fed from a 100V variable frequency source. Find i) frequency at which current is maximum ii) impedance at this frequency and iii) voltage across inductance at this frequency.
14. A series RLC circuit consists of R=100 ohm, L = 0.02 H and C = 0.02 microfarad. Calculate frequency of resonance.
A variable frequency sinusoidal voltage of constant RMS value of 50V is applied to the circuit. Find the frequency at which voltage across L and C is maximum. Also calculate voltage across L and C is maximum. Also calculate voltages across L and C at frequency of resonance. Find maximum current in the circuit.
15. In the parallel RLC circuit, calculate resonant frequency, bandwidth, Q-factor and power dissipated at half power frequencies.

B. Two Port Networks

1. For the network of Fig. 7.69, find z-parameters. Hence find y-parameters, Find whether the network is Reciprocal and symmetrical.

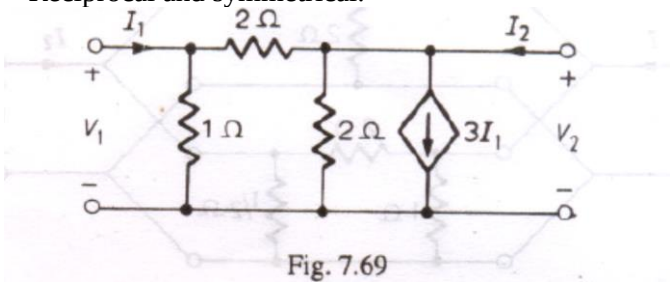


Fig. 7.69

2. For the network of Fig. 7.70, find y-parameters. Hence find z-parameters. Find whether the network is reciprocal and symmetrical

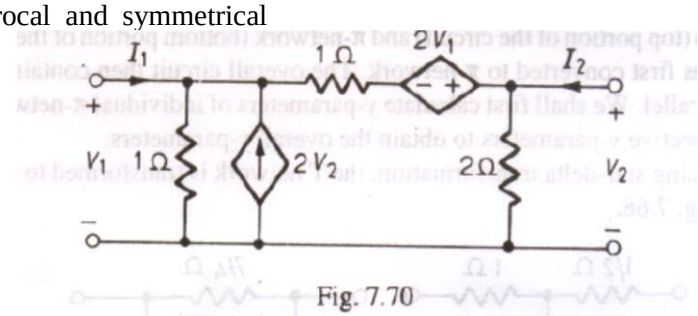


Fig. 7.70

3. For the network of Fig. 7.71 find the h-parameters. Hence find g-parameters. Find whether the network is reciprocal and symmetrical.

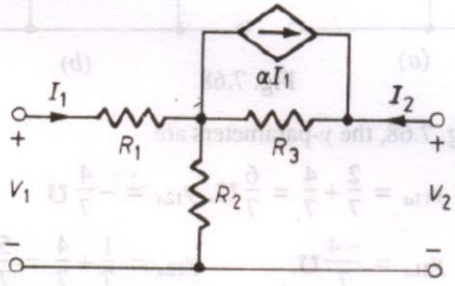


Fig. 7.71

4. For the network shown in Fig. 7.72 find the transmission *(ABCD)* parameters. Find whether the network is reciprocal and symmetrical.

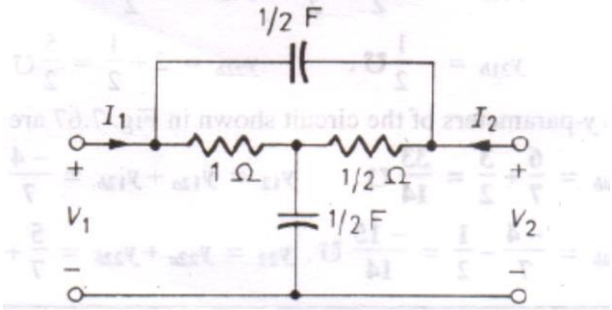


Fig. 7.72

5. The z-parameters of a certain two-port network are Z_{ll}=5 , Z_{12}=Z_{21} =3 ,Z_{22}=4. Find
   (a) ABCD parameters (b)abcd parameters (c)h parameters (d) g parameters.
6. The transmission (ABCD) parameters of a certain two-port network are A = 1,B = 2,C = 1 and D = 3.
7. Calculate (a) z-parameters (b) h-parameters. Is the network (i) reciprocal (ii) symmetrical?
8. A symmetrical lattice network has series arm impedance of 5 ohm and cross-arm impedance of 10Ohm.
   Find (a) z-parameters (b) image parameters.
9. For the network shown in Fig. 7.73, find (a) h-parameters (b) ABCD parameters (c) z-parameters.

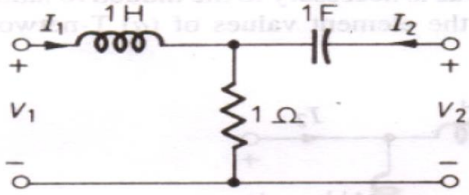


Fig. 7.73

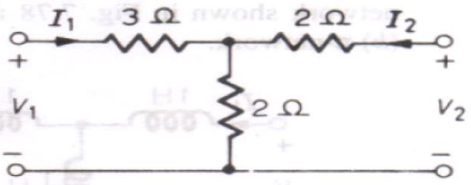


Fig. 7.74

10. Starting from fundamentals calculate the Network parameters of the network shown in Fig. 7.74.

11. Obtain the y-parameters of the network shown in Fig. 7.75 considering it as a parallel combination of two circuits.

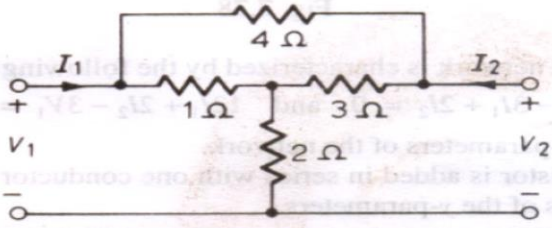


Fig. 7.75

12. For the network shown in Fig. 7.77, calculate the y-parameters.

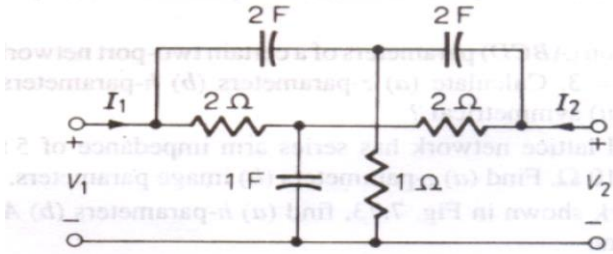


Fig. 7.77

13. (a) A two-port network is characterized by the following equations

$$6V_1 - 3I_1 + 2I_2 = 0 \quad \text{and} \quad 12I_1 + 2I_2 - 3V_1 = 5V_2$$

Find the y-parameters of the network.
(b) A 5-il resistor is added in series with one conductor to the output port. Find new values of the y-parameters.

14. The block N of the network shown in Fig. 7.79 has following z-parameters :

$$z_{11} = 0.1\ \text{k}\Omega,\ z_{12} = -0.5\ \text{k}\Omega,\ z_{21} = 1\ \text{k}\Omega,\ z_{22} = 10\ \text{k}\Omega.$$

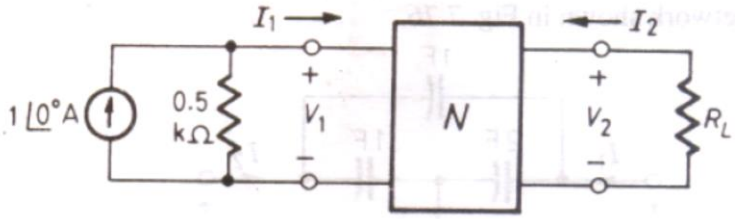


Fig. 7.79

a. Find the r m s value of voltage across R_L if R_L=5 kΩ
b. Find the optimum value of R_L which would result in maximum power being delivered to it.
c. Find the y-parameters of the block N.

15. Find the z-parameters of the network shown in Fig. 7.80.

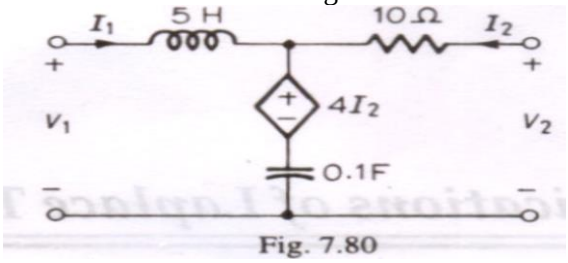


Fig. 7.80

16. The two-port network *N* shown in Fig. 7.81 has following h-parameters :

$$h_{11} = 1\ \text{k}\Omega,\ h_{12} = 0.0015,\ h_{21} = 100,\ h_{22} = 100\ \mu\text{℧}.$$

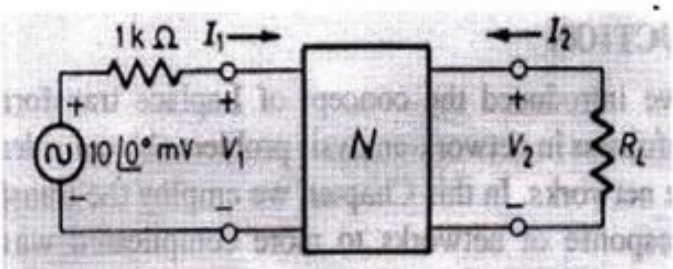


Fig. 7.81

(a) Find the output voltage V_2 if R_L = 10 k ohm.
(b) Find R_L which would result in maximum power being delivered to it.
(c) Find z-parameters of the two port network N.

17. Determine the input impedance Z_{in} of a two-port network, if a load resistor of 4 ohm is connected across its output port. The z-parameters of the network are

$$z_{11} = 5\ \Omega,\ z_{12} = z_{21} = 3\ \Omega,\ z_{22} = 2\Omega$$

18. The network equations for a two-port network give the currents I_1 and I_2 at the two ports as

$$I_1 = 0.25V_1 - 0.2V_2 \quad \text{and} \quad I_2 = -0.2V_1 + 0.1V_2$$

Determine the transmission *(ABCD)* parameters for the network and hence write the network equations Using these parameters.

19 . For the resistive network shown in Fig. 7.82, calculate the y-parameters.

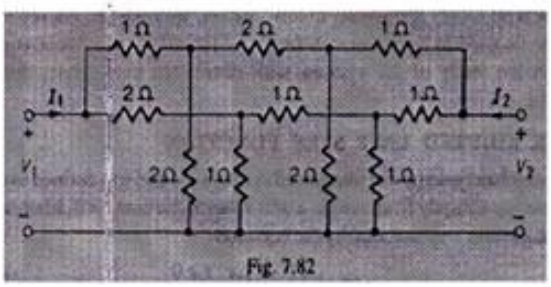


Fig. 7.82

Examination	S+	S	A	B	C	D	E	F	% Passing
Mar-2021	-	-	-	-	-	-	-	05	83.33

Prepared by	Checked by		
Prof.P.V.Patil	Prof.D.M.Kumbhar	HOD	Principal

Subject Title	**Electronic Devices**		
Subject Code	18EC33	**CIE Marks**	40
Number of Lecture Hrs /	03	**SEE Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. D. M. Kumbhar	**Designation:** Asst. Professor	**Experience: 14.0**
No. of times course taught:02	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I/II	Basic Electronics Engg. Physics

2.0 Course Objectives

This course will enable students to:

1. Understand the basics of semiconductor physics and electronic devices.
2. Describe the mathematical models BJTs and FETs along with the constructional details.
3. Understand the construction and working principles of optoelectronic devices
4. Understand the fabrication process of semiconductor devices and CMOS process integration

3.0 Course Outcomes

	Course Outcome	RBT Levels	POs
C203.1	Understand the principles of semiconductor Physics	**L1& L2**	1,2,3,4,10,12
C203.2	Understand the principles and characteristics of different types of semiconductor devices	**L1& L2**	1,2,3,4,10,12
C203.3	Utilize the mathematical models of transistor for circuits and systems.	**L1& L2**	1,2,3,4,10,12
C203.4	Utilize the mathematical models of MOS transistors for circuits and systems.	**L1& L2**	1,2,3,4,10,12
C203.5	Understand the fabrication process of semiconductor devices	**L1& L2**	1,2,3,4,10,12
Total Hours of instruction			**40**

4.0 Course Content

MODULES	RBT Levels	No. Of Hours
MODULE-I Semiconductors Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. **(Text 1: 3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.2.1, 3.2.3, 3.2.4, 3.4.1, 3.4.2, 3.4.3, 3.4.5).**	**L1& L2**	**8**
MODULE-II P-N Junctions Forward and Reverse biased junctions- Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers. **(Text 1: 5.3.1, 5.3.3, 5.4, 5.4.1, 5.4.2, 5.4.3)** Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photo detectors. Light Emitting Diode: Light Emitting materials**.(Text 1: 8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1)**	**L1& L2**	**8**
MODULE-III Bipolar Junction Transistor Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown. **(Text 1: 7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3).**	**L1& L2**	**8**
MODULE-IV Field Effect Transistors Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics. **(Text 2: 9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1,** 9.8.2).	**L1& L2**	**8**
MODULE-V Fabrication of p-n junctions Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. **(Text 1: 5.1)** **Integrated Circuits: Background**, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements**. (Text 1: 9.1, 9.2, 9.3.1, 9.3.3).**	**L1& L2**	**8**

5.0 Relevance to future subjects

Sl. No.	Semester	Subject	Topics
1.	IV	Analog Electronics	**All Modules**
2.	VI	Nano electronics	Module-3 Fabrication techniques:

6.0 Relevance to Real World

SL. No.	Real World Mapping
01	Learnt methods are used to solve some computer related problems.
02	Accessing I/O devices, interfacing and Working with principles of memory system.
03	Designing the arithmetic and logical operations

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Ebers-Moll Model
02	NPTEL	Neil Bohr's Atomic Model

8.0 Books Used and Recommended to Students

Text Books
1.Ben. G. Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices", 7thEdition, Pearson Education, 2016, ISBN 978-93-325-5508-2. 2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition, MCGraw Hill Education, 2012, ISBN 978-0-07-107010-2
Reference Books
1. 1. S. M. Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd Edition, Wiley, 2018. 2. A. Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI, 1993.
Additional Study material & e-Books
2. Nil

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
1. https://nptel.ac.in/courses/113106062/30 2. https://nptel.ac.in/courses/108108112/ 3. https://www.youtube.com/watch?v=VOSvTbKId9M&list=PLbNbEKpZSUoQKBqJQcsvPB2yE_rQeKD3E&index=1 4. https://www.youtube.com/watch?v=eO6kktZGmOY&list=PLbNbEKpZSUoQKBqJQcsvPB2yE_rQeKD3E&index=4

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	The physics of semiconductor devices	https://ieeexplore.ieee.org/document/1069942
2	American Journal of Physics	https://aapt.scitation.org/doi/10.1119/1.1969398
3	Semiconductors: Materials, Physics, and Devices	https://www.hindawi.com/journals/apec/si/485324/cfp/

11.0 Examination Note

Internal Assessment: 40 Marks

Theoretical aspects as well as relevant sketches should be drawn neatly.

Scheme of Evaluation for Internal Assessment (40 Marks)

(c) Internal Assessment test in the same pattern as that of the main examination (All the three Internal Tests marks considered): **30**Marks.

(d) Assignments: **10** Marks

SCHEME OF EXAMINATION:

Question paper pattern:

Note: - The SEE question paper will be set for 100 marks and the marks will be proportionately reduced to 60.

6. The question paper will have **ten** full questions carrying equal marks.
7. Each full question consisting of **20** marks.
8. There will be **two** full questions (with a **maximum** of **four** sub questions) from each module.
9. Each full question will have sub question covering all the topics under a module.
10. The students will have to answer **five** full questions, selecting **one** full question from each module.

12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
MODULE-1 Semiconductors	1	Bonding forces in solids	**20**
	2	Energy bands	
	3	Metals, Semiconductors and Insulators,	
	4	Direct & Indirect semiconductors and Electrons and Holes	
	5	Intrinsic and Extrinsic materials	
	6	Conductivity and Mobility & Drift and Resistance	
	7	Effects of temperature and doping on mobility	
	8	Hall Effect	
MODULE-2 P-N Junctions	9	Forward and Reverse biased junctions-	**20**
	10	Qualitative description of Current flow at a junction	
	11	reverse bias, Reverse bias	
	12	Breakdown- Zener breakdown, avalanche breakdown	
	13	Rectifiers	
	14	Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction	
	15	Solar Cells, Photo detectors	
	16	Light Emitting Diode: Light Emitting materials	
MODULE-3 Bipolar Junction Transistor	17	Fundamentals of BJT operation	**20**
	18	Amplification with BJTS and BJT Fabrication	
	19	The coupled Diode model (Ebers-Moll Model),	
	20	Switching operation of a transistor and Cutoff saturation	
	21	switching cycle	
	22	specifications	
	23	Drift in the base region, Base narrowing	
	24	Avalanche breakdown	
MODULE-4 Field Effect Transistors	25	Basic pn JFET Operation	**20**
	26	Equivalent Circuit and Frequency Limitations	
	27	MOSFET Two terminal MOS structure	
	28	Energy band diagram	
	29	Ideal Capacitance – Voltage Characteristics and Frequency Effects	
	30	Basic MOSFET Operation	
	31	MOSFET structure	
	32	Current-Voltage Characteristics	
MODULE-5 Fabrication of p-n junctions	33	Thermal Oxidation and Diffusion	**20**
	34	Rapid Thermal Processing	
	35	Ion implantation	
	36	Chemical vapor deposition	

	37	Photolithography and Etching, metallization	
	38	**Integrated Circuits** : Evolution of ICs	
	39	CMOS Process Integration	
	40	Integration of Other Circuit Elements	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity.	Book 1, of the text. Website of the Reference list
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity.	Book 1 of the text. Website of the Reference list
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity.	Book 1 of the text. Website of the Reference list
4	Assignment 4: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity.	Book 2 of the text. Website of the Reference list
5	Assignment 5: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	10	Individual Activity.	Book 2 of the text. Website of the Reference list

14.0 QUESTION BANK

MODULE-1

1. Explain bonding forces in solids
2. Metals, Semiconductors and Insulators
3. Differentiate Direct & Indirect semiconductors
4. Explain Intrinsic and Extrinsic semiconductor materials
5. Explain Effects of temperature and doping on mobility
6. Explain Hall Effect
7. Explain Drift and Resistance
8. Explain Energy bands
9. Explain Conductivity and Mobility.

MODULE -2

1. Explain Forward and Reverse biasing of pn junction
2. Explain Qualitative description of Current flow at a junction
3. Differentiate Zener breakdown and avalanche breakdown
4. Explain Photodiodes Current and Voltage characteristics.
5. Explain Solar Cell and Photo detector.
6. Explain Light Emitting Diode.
7. With nest sketch explain bridge and center tapped rectifiers.

MODULE -3

1. With a neat diagram explain the. BJT operation
2. Explain BJT Fabrication
3. Explain the coupled Diode model of transistor (Ebers-Moll Model),
4. Explain switching operation of a transistor.
5. Explain Cutoff and saturation regions of transistor.
6. Explain drift in the base region and base narrowing

MODULE -4

1. Explain pn n-Channel JFET Operation
2. Differentiate JFET and MOSFET
3. Explain MOS structure and Energy band diagram
4. Explain Basic MOSFET Operation.
5. Explain n- Channel MOSFET structure.

MODULE -5

1. Explain Thermal Oxidation and Diffusion.
2. Explain Rapid Thermal Processing.
3. Explain Ion implantation.
4. Explain Photolithography and Etching, metallization.
5. Explain CMOS Process Integration.

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15.0 University Result

Examination	S+	S	A	B	C	D	E	% Passing
Dec-2018/Jan-2019	--	1	5	7	18	2	--	97.01
Dec 2019/Jan2020		1	11	7	6	-	-	83.33

Prepared by	Checked by		
Prof.D.M.Kumbhar	Prof.S.B.Akkole.	HOD	Principal

Subject Title	DIGITAL SYSTEM DESIGN		
Subject Code	18EC34	**CIE Marks**	40
Number of Lecture Hrs / Week	03	**SEE Marks**	60
Total Number of Lecture Hrs	40 (08 Hours per Module)	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof D.B.Madihalli	**Designation:** Assistant Professor	**Experience:**14 yrs
No. of times course taught:07	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I / II	BASIC ELECTRONICS

2.0 Course Objectives

This course will enable students to:

- Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine- McClusky Techniques.
- Design combinational logic circuits.
- Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- Describe Latches and Flip-flops, Registers and Counters.
- Analyze Mealy and Moore Models.
- Develop state diagrams Synchronous Sequential Circuits.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	RBT Level	POs
C204.1	Explain the concept of combinational & sequential circuits.	L1,L2,L3	PO1,2,3,4,5,6,12
C204.2	Analyze & Design the combinational logic circuits.	L1,L2.L3	PO1,2,3,4,5,6,12
C204.3	Describe & Characterize flip-flops & its applications.	L1.L2.L3	PO1,2,3,4,5,6,12
C204.4	Design the sequential circuits using SR, JK, D, T flip-flop and Mealy & Moore machines.	L1.L2.L3	PO1,2,3,4,5,6,12
C204.5	Design applications of combinational & sequential circuits.	L1.L2.L3	PO1,2,3,4,5,6,12
Total Hours of instruction		**40**	

4.0 Course Content

Course Content:

Module 1: Principles of combination logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms), Simplifying Max term equations, Quine-McCluskey minimization techniques – 3 & 4 variables.(Text 1, Chapter 3). **L1, L2, L3**

Module 2: : Analysis and design of combinational logic: Decoders, Encoders, digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators (Text 1, Chapter 4) Programmable Logic Devices, Complex PLD, FPGA. (Text 3- Chapter 9,9.6 to 9.8) . **L1, L2, L3**

Module 3: Flip-Flops & its applications: BasicBistableelements,Latches,The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, Characteristicequations, Registers, binary ripple counters and synchronous binary counters.
(Text2,Chapter6)**L1, L2, L3**

Module 4: Sequential Circuit Design: Design of a synchronous counters, Design of a synchronous mod-n counter using clocked JK , D, T and SR flip-flops. (Text 2 - Chapter6). **L1, L2, L3**
Mealy and Moore models, state machine notation, construction of state diagrams.(Text 1 – chapter 6)

Module 5: Applications of digital circuits: Design of sequence detector, guidelines for construction of state graphs, design example – code converter, design of iterative circuits (comparator), design of sequential circuits using ROM & PLA's, CPLD's and FPGAs, serial adder with accumulator, design of binary multiplier, design of binary divider.
(Text 3 – 14.1,14.3,16.2,16.3,16.4,18.1,18.2,18.3) **L1, L2, L3**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Embedded System

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Analyze different types of digital circuits in digital systems.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Multisim Simulation in digital electronics lab

8.0 Books Used and Recommended to Students

Text Books
1. DigitalLogicApplicationsandDesign,JohnMYarbrough,ThomsonLearning, 2001. 2. DonaldD.Givone,—DigitalPrinciplesandDesign,McGrawHill,2002. 3. Charles H Roth Jr., Larry L. Kinney – Fundamentals of logic design, Cengage Learning, 7th edition.
Reference Books
1. D.P.KothariandJ.SDhillon,—DigitalCircuitsandDesign,Pearson,2016. 2. Morris Mano, —Digital Design, Prentice Hall of India, Third Edition. 3. K. A. Navas, —Electronics Lab Manual, Volume I, PHI, 5th Edition, 2015.
Additional Study material & e-Books
1. NPTEL notes and Videos 2. VTU Online notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
03) https://nptel.co.in

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Explorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of three will be accounted.

Scheme of Evaluation for Internal Assessment (40 Marks)
(e) 30 marks for IA Test & 10 marks for Assignment.

SCHEME OF EXAMINATION:
Four questions to be set from the syllabus covered.
Question 1 or 2 and Question 3 or 4. Answer any two main questions.
Question 1 or 2 = 15 marks.
Question 3 or 4 = 15 marks.

Total = 30 Marks

12.0 Course Delivery Plan

Course Delivery Plan:

Module	Lecture No.	Content of Lecture	% of Portion
1	1	Design of Combinational Logic Circuit.	20
	2	Canonical Forms.	
	3	Generation of Switching equations from truth table.	
	4	Karnaugh Maps – 3,4 Variables.	
	5	Karnaugh Map with Don't Care Conditions.	
	6	Simplifying Maxterm equations.	
	7	Five Variables Karnaugh Map.	
	8	Quine- McCluskey Minimization Technique.	
2	9	Decoders & Encoders.	40
	10	Digital Multiplexers.	
	11	Using multiplexers as Boolean function generators.	
	12	Adders & Subtractors.	
	13	Look Ahead Carry Generator.	
	14	Binary Comparators.	
	15	Programmable logic devices	
	16	Complex PLD, FPGA	
3	17	Basic Bistable Element.	60
	18	SR Latch: SR Latch using NOR Gates , Gated SR Latch using NOR Gate.	
	19	SR Latch using NAND Gates , Gated SR Latch using NAND Gate.	
	20	Pulse Triggered flip-flops : Clocked SR flip-flop & Edge Triggered Flip-flops.	
	21	Clocked D , JK , T flip-flop & Master Slave SR flip-flop, Master slave JK flip-flop.	
	22	Characteristics equations of SR , JK , D , T flip-flops	
	23	Registers & Binary ripple counters.	
	24	Synchronous binary counters.	
	25	Introduction, Design of Synchronous Counter, Modulus-N	

4		Synchronous Up Counter	80
	26	Modulus-N Synchronous Down Counter , Up/Down Counter	
	27	Design of Mod N counter using T , JK flip-flop.	
	28	Design of Mod N counter using SR, D flip-flop.	
	29	Ring Counter, Johnson Counter.	
	30	Introduction to Moore Model & Mealy Model	
	31	State Machine Notations & Synchronous Sequential Circuit Analysis	
	32	Construction of state diagrams & Counter Design	
5	33	Design of sequence generator.	100
	34	Guidelines for construction of state graphs.	
	35	Design example – code converter.	
	36	Design of iterative circuits (comparator).	
	37	Design of sequential circuits using ROM & PLA's.	
	38	CPLD's and FPGAs.	
	39	Serial adder with accumulator.	
	40	Design of binary multiplier, design of binary divider.	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on principles of combinational logic	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1	2	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
2	Assignment 2: University Questions on analysis & design of combinational logic	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2	4	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions on flip flops and its applications.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3	6	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
4	Assignment 4: University Questions on sequential circuit design.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4	8	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions on sequential circuit design.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5	12	Individual Activity. Printed solution expected.	Book 1, 2 of the reference list. Website of the Reference list
6	Mini Project Rivets based for the students groups	Students study the Rivets applications from Real World Example view.	Syllabus with Real World Mapping	16	Group Activity. Student Group need to perform Project and do a brief Report	All Books / paper Resources / Study Material. All Internet / Web resources.

14.0 Assignment Questions

Assignment No	Questions	Marks
I	1. M = f (W,X,Y,Z) = ∑ (1,4,5,6,11,12,13,14,15) Simplify using k-map & realize NAND gate. 2. Y = f (a,b,c,d) = ∑ (0,2,3,5,8,10,11) simplify using Quine-McCluskey method. 3. Convert the given Boolean expression into a) Y = f(a,b,c) = (a+b) (a+c) minterm canonical form. b) P = f(a,b,c) = (a+b) (b+c) (c+a) maxterm canonical form. 4. F(a,b,c,d) = πM (0,2,6,11,13,15 + dc(1,9,10,14) find the minimal sum & minimal product. 5. Obtain the SOP using QM method of f (w,x,y,z) = ∑m (7,9,12,13,14,15) + dc(4,11).	5marks for each
II	1. Implement the given functions using IC 74138 a) P = f1 (X,Y,Z) = ∑ (1,2,5,6) b) Q = f2(X,Y,Z) = π (3,5,6,7) 2. Design & Implement 4 – bit look ahead carry adder. 3. Design & Implement BCD to Excess-3 code converter. 4. Explain Complex PLD & FPGA. 5. Explain carry look ahead adder with neat circuit diagram & relevant expressions.	5marks for each
III	1. Explain the working principle of gated SR latch. 2. Explain the working of master slave JK flip flop with the help of logic diagram , function table , logic symbol & timing diagram. 3. Explain the working of positive edge triggered D flip flop. 4. Derive the characteristics equation for JK & T flip flop. 5. Explain registers & binary counters.	5marks for each
IV	1. Design synchronous mod – 6 counter using clocked T flip flop. 2. Explain mod – 4 ring counter using D flip flop. 3. Explain Mealy & Moore sequential circuit models. 4. Define the terms : input variable , output variable , Excitation table , state variable. 5. What is state table. Give an example.	5marks for each
V	1. Explain the design of sequence generator. 2. Explain the design of sequential circuits using ROMs & PLAs. 3. Explain serial adder with accumulator. 4. Explain the design of binary multiplier. 5. Explain the design of binary divider.	5marks for each

15.0 QUESTION BANK

Module 1 : Principles of combinational logic

1. Draw a model representing combinational circuits. Label the input & output variables. Write a general expressions showing the input & output relationship.
2. Describe what is mean by combinational logic in your own words.
3. How does a "truth table" express a combinational circuit?
4. Construct a truth table & write the Boolean output equations for the following verbal problem statements-
   a. A single output variable, Z, is to be true when the input variables a and b true and when b is false but a and c are true.
   b. An output is to be true (logical 1) when the value of the inputs exceeds 3. The weighting for each input variable is as follows: w=3 x = 3 y =2 z = -1
5. Convert the following equations into their requested canonical forms:
   a. (SOP) X = a'b + bc
   b. (POS) P = (w' + x) (y + z')
   c. (SOP) T = p(q' + s)
   d. (SOP) R = L + M'(N'M + M'L)
   e. (POS) U = r' + s(t + r) + s't

6. Simplify the following using Karnaugh maps:
    a. X = a'bc + ab'c' + abc
    b. Y= f(a, b, c) =Σ(1, 3, 5, 6, 7)
    c. T = w'xy + wz' + xyz'
    d. P = f(w, x, y, z) = Σ(0, 2, 8, 10)
7. Convert the given Boolean function f(x, y, z) = [x + xz (y + z)] into maxterm canonical formula and hence highlight the importance of canonical formula.
8. Distinguish the prime implicants and essential prime implicants. Determine the same of the function f(w, x, y, z) = Σ m(0, 1, 4, 5, 9, 11, 13, 15)
9. Design a combinational logic circuit, which converts BCD code into Excess – 3 code and draw the circuit diagram.
10. Simply the following noncanonical expressions using Karnaugh maps:
    a. T = a'b'c'de + a'bc'de + abcde + ab'c'de
    b. P = v'w' + v'wy' + vw'z
    c. G = y'z + w'xy' + w'xy + xy'z
11. Using Quine – Mcluskey method and prime implicant reduction table, obtain the minimal sum expression for the Boolean function f(w, x, y, z) = Σ m(1, 4, 6, 7, 8, 9, 10, 11, 15).
12. Obtain the minimal product of the following Boolean functions using QM technique: f(w, x, y, z) = Σ m(1, 5, 7, 10, 11) + dc(2, 3, 6, 13)

Module 2 : Analysis & Design of combinational logic

1. Shortly explain the decoder.
2. Design 4:16 decoder using two 3:8 decoder.
3. Design 5:32 decoder using one 2:4 & four 3:8 decoder IC's.
4. Explain realization of multiple output function using Binary decoder.
5. Implement following function using 3:8 decoder – f1(A,B,C) = m(1,4,5,7) and f2(A,B,C) = M(2,3,6,7).
6. Design combinational circuit of BCD to 7 segment display using decoder.
7. Write short note on – encoder.
8. Design keypad interface to digital system using 10 lines to BCD encoder.
9. Design octal to binary encoder.
10. Briefly explain priority encoder.
11. Design 32:5 priority encoder using four 74LS148 & gates.
12. Implement full adder & full substractor using decoder & write its truth table.
13. Write short note on – multiplexer and de-multiplexer.
14. Design 32:1 MUX using two 74LS150 ICs.
15. Design 32:1 MUX using four 8:1 MUX & 2:4 decoder.
16. Implement following functions using 4:1, 8:1 & 16:1 MUX - f1(A,B,C,D) = Σ m(0,1,2,4,6,9,12,14) and f2(A,B,C,D) =Σ m(0,1,3,4,8,9,15).
17. Implement following expression – F(A, B, C, D) = ABD + ACD + BCD + ACD using 8:1 MUX.
18. Construct 8:1 MUX using 2:1 MUX.
19. Implement full adder & full substractor using DeMUX.
20. Explain the concept of carry look ahead adder. Design 4-bit carry look ahead circuit.
21. Design 2-bit comparator.
22. Explain full adder & full substractor circuit.
23. Explain the programmable logic devices.
24. Explain the complex PLD and FPGA.

Module 3 : Flip-Flops & its applications

1. Explain the difference between combinational & sequential circuits.
2. Explain the difference between synchronous & asynchronous sequential circuits.
3. Explain the operation of SR Flip Flop.
4. Explain the working of switch Debouncer using SR latch.
5. Explain SR latch using NOR gate & Gated SR latch using NOR & NAND gate.
6. Explain Characteristics of SR Latch & its state Transition Diagram.
7. Explain the race around condition in detail. How it is eliminated?
8. Draw the master slave SR flip – flop. Explain flip-flop action during control signal & also give the truth table.
9. Draw & explain master slave JK flip-flop.
10. Explain JK , T & D-flip-flop.
11. Draw & explain edge triggered flip-flop.
12. Convert SR flip flop to JK flip flop.

13. Explain Left shift serial in serial out register with D flip flop.
14. Explain serial in parallel out shift register.
15. Explain parallel in serial out shift register.
16. Explain Ring counter & Johnson Counter.
17. Explain binary ripple counters.
18. Explain synchronous binary counter.

Module 4 : Sequential Circuit Design

1. Explain modulus - 4 synchronous up counter using JK F/F.
2. Explain modulus - 4 synchronous down counter .
3. Explain modulus - 4 synchronous up / down counter.
4. Explain modulus - 8 synchronous up D F/F counter.
5. Explain modulus - 8 synchronous down counter.
6. Explain modulus - 8 synchronous up / down counter.
7. Explain state table, transition table, exaltation table.
8. Construct Mealy state diagram that will detect a serial sequence of 10110. When the input pattern has been detected, cause an output Z to be asserted high.
9. Explain the analysis of asynchronous sequential circuit.
10. Explain fundamental mode asynchronous sequential circuit without latches.
11. Explain pulse mode asynchronous sequential circuit with latches.
12. Write the difference between Mealy & Moore Models.

Module 5 : Applications of digital circuits

1. Explain the design of sequence generator.
2. Explain the design of sequential circuits using ROMs & PLAs.
3. Explain serial adder with accumulator.
4. Explain the design of binary multiplier.
5. Explain the design of binary divider.

16.0 University Result

Examination	S+	S	A	B	C	D	E	F	% Passing
Dec 2019/Jan2020	00	1	10	9	8	2	2	2	94.11
Dec 2020/Jan2021	00	00	10	12	05	01	00	01	96.67

Prepared by	Checked by		
Prof.D.B.Madihalli	Prof.S.B.Akkole.	HOD	Principal

Subject Title	**Computer Organization and Architecture**		
Subject Code	18EC35	**CIE Marks**	40
Number of Lecture Hrs /	03	**SEE Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03
		CREDITS – 03	

FACULTY DETAILS:		
Name: Prof. **B. P. Khot**	**Designation:** Asst. Professor	**Experience: 5.9 Years**
No. of times course taught: 01	**Specialization:** Microelectronics and control systems	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I/II	CCP

2.0 Course Objectives

This course will enable students to:

5. Explain the basic sub systems of a computer, their organization, structure and operation.
6. Illustrate the concept of programs as sequences of machine instructions.
7. Demonstrate different ways of communicating with I/O devices
8. Describe memory hierarchy and concept of virtual memory.
9. Illustrate organization of simple pipelined processor and other computing systems

3.0 Course Outcomes

CO No.	Course Outcome	RBT Levels	POs
C205.1	Explain the basic organization of a computer system.	L1, L2 & L3	1,2,3,8,10,12
C205.2	Explain different ways of accessing an input / output device including interrupts	L1, L2 & L3	1,2,3,8,10,12
C205.3	Illustrate the organization of different types of semiconductor and other secondary storage memories	L1, L2 & L3	1,2,3,8,10,12
C205.4	Illustrate simple processor organization based on hardwired control and micro programmed control.	L1, L2 & L3	1,2,3,8,10,12
C205.5	Illustrate simple processor organization based on hardwired control and micro programmed control.	L1, L2 & L3	1,2,3,8,10,12
		Total Hours of instruction	**40**

4.0 Course Content

MODULES	RBT Levels	No. of Hours
MODULE-I **Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation (up to 1.6.2 of Chap 1 of Text). **Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing (upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).	**L1, L2 & L3**	**08**
MODULE-II Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of Text).	**L1, L2 & L3**	**08**
MODULE-III **Input/Output Organization**: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access (up to 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text).	**L1, L2 & L3**	**08**
MODULE-IV **Memory System:** Basic Concepts, Semiconductor RAM Memories Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks (5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text**)**	**L1, L2 & L3**	**08**
MODULE-V **Basic Processing Unit:** Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Micro programmed Control (upto 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text	**L1, L2 & L3**	**08**

5.0 Relevance to future subjects

Sl. No.	Semester	Subject	Topics
1.	IV	Microprocessor	Bus Structures , Input/output Organization, Memory System, Arithmetic and Basic Processing Unit
2.	V	Operating Systems	Basics of Operating Systems

6.0 Relevance to Real World

SL. No.	Real World Mapping
01	Learnt methods are used to solve some computer related problems.
02	Accessing I/O devices, interfacing and Working with principles of memory system.
03	Designing the arithmetic and logical operations

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Seminar on basics of computer Architecture
02	NPTEL	Study on hardware parts of a computer

8.0 Books Used and Recommended to Students

Text Books
20. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.
Reference Books
1. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009. **2.** William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006. **3.** Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.
Additional Study material & e-Books
3. Fundamentals of Computer organization and Design *by Shivarama Dandamud* 4. Fundamentals of Computer Organization and Architecture *by Barr and Rewini* 5. Computer Organization by ISRD Group

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
5. https://en.wikibooks.org/wiki/IB/Group_4/Computer/Computer_Organisation 6. nptel.ac.in/courses/106106092/ 7. nptel.ac.in/courses/106103068/ 8. www.cse.iitm.ac.in/~vplab/courses/comp_org.htm 9. https://www.youtube.com/playlist?list=PLWPirh4EWFpF0FVeBgL75d1RlASn4sGoz

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IJCOT - International Journal of Computer & Organization Trends	www.ijcotjournal.org/
2	Journals - The Science and Information (SAI) Organization	thesai.org/Publications
3	Computer Hardware Organizations Innovate with IEEE Information	https://www.ieee.org/documents/ieee_focus_on_computer_hardware.pdf

11.0 Examination Note

Internal Assessment: 40 Marks

Theoretical aspects as well as relevant sketches should be drawn neatly.

Scheme of Evaluation for Internal Assessment (40 Marks)

(f) Internal Assessment test in the same pattern as that of the main examination (All the three Internal Tests marks considered): **30**Marks.

(g) Assignments: **10** Marks

SCHEME OF EXAMINATION:

Question paper pattern:

Note: - The SEE question paper will be set for 100 marks and the marks will be proportionately reduced to 60.

1. The question paper will have **ten** full questions carrying equal marks.
2. Each full question consisting of **20** marks.
3. There will be **two** full questions (with a **maximum** of **four** sub questions) from each module.
4. Each full question will have sub question covering all the topics under a module.
5. The students will have to answer **five** full questions, selecting **one** full question from each module.

12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
MODULE-1	1	Computer Types and Functional Units	20
	2	Basic Operational Concepts	
	3	Bus Structures	
	4	Software, Performance – Processor Clock	
	5	Basic Performance Equation, Numbers,	
	6	Arithmetic Operations and Characters	
	7	Machine Instructions and Programs	
	8	Floating point Numbers, IEEE standard for Floating point Numbers	
	9	Memory Location and Addresses	
	10	Memory Operations Instructions and Instruction Sequencing	
MODULE-2	11	Addressing Modes,	20
	12	Cont'd Addressing Modes	
	13	Cont'd Addressing Modes	
	14	Assembly Language	
	15	Basic Input and Output Operations	
	16	Stacks and Queues	
	17	Subroutines	
	18	Additional Instructions	
MODULE-3	19	Accessing I/O Devices,	20
	20	Cont'd … Accessing I/O Devices	
	21	Interrupts – Interrupt Hardware,	
	22	Enabling and Disabling Interrupts	
	23	Handling Multiple Devices	
	24	Controlling Device Requests	
	25	Cont'd… controlling device requests	
	26	Direct Memory Access	
MODULE-4	27	Basic Concepts	20
	28	Semiconductor RAM Memories	
	29	Internal organization of memory chips	
	30	Static memories	
	31	Asynchronous DRAMS,	
	32	Read Only Memories	
	33	Cash Memories	
	34	Virtual Memories	
	35	Secondary Storage-Magnetic Hard Disks	

MODULE-5	36	Some Fundamental Concepts, , Multiple Bus Organization, ,	**20**
	37	Execution of a Complete Instruction	
	38	Multiple Bus Organization	
	39	Hardwired Control	
	40	Multiple Bus Organization	
	41	Hardwired Control	
	42	Microprogrammed Control	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity.	Book 1, of the reference list. Website of the Reference list
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	6	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
4	Assignment 4: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	8	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list
5	Assignment 5: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	10	Individual Activity.	Book 1, 2 of the reference list. Website of the Reference list

14.0 QUESTION BANK

MODULE-1

10. With a neat diagram discuss the basic operational concept of a computer.
11. Explain methods to improve the performance of computer.
12. Explain Big-Endian, little Endian and assignment byte addressability
13. What are the addressing modes? Explain the different 4 types of addressing modes with examples.
14. Write the use of Rotate and shift instruction with example

15. What is stack and queue? Write the line of code to implement the same.
16. Explain the following for a computer MAR, MDR, PC ALU, and Control unit.
17. Explain the operation of two bus structure.
18. Explain Cleary SPEC rating and its significance
19. Briefly explain the history of computer development from First generations to 4 the Generation
20. Mention the diff between CISC and RISC processors.
21. Explain with examples, all the generic addressing modes, with assembler syntax.
22. Mention the differences between CISC and RISC processors.
23. Differentiate between stack and queue
24. Define.
    i) Memory Latency
    ii) Memory bandwidth
    iii) Hit-rate
    iv) Miss-penalty
25. Explain the representation of Floating point numbers using IEEE Format.
26. Perform following operations on the 5-bit signed numbers using 2's compliment representation system. Also indicate overflow has occurred.
    i) (-9) + (-7) ii) (+7) - (-8).
27. Explain I/O mapped I/O and describe any two methods of connecting multiple interrupting devices to CPU
28. Explain with a neat block diagram, 4 bit carry look ahead adder.
29. Explain the concept of carry save addition for the multiplication operation, MxQ=P for 4-bit operands with diagram and suitable example.
30. Multiply the following signed 2's complement numbers using Booth's algorithm multiplicand = $(010111)_2$, multiplier = $(110110)_2$
31. Perform division operation on he following unsigned numbers using the restoration method. Dividend = $(10101)_2$, divisor = $(00100)_2$.
32. With a neat diagram explain the floating point addition/ subtraction unit.
33. Describe the organization of 64*8 memory using 16*1k static memory chips

MODULE -2

1. Describe any three modes of addressing.
2. Write a program to evaluate the Expression S=A*B+C*D
3. What are the diff types of addressing modes?
4. What is word alignment of a machine explain what are the consecutive addresses of aligned words for 16, 32 and 64.
5. Bring out the five key differences between subroutine and interrupt service routine.
6. 80what is the function of assembler directives? give two examples of assembler directives used for the reservation for memory locations for variables, state their functions.
7. Define an addressing mode explain the following addressing modes with examples: Indirect, indexed, relative and auto increment.
8. Explain how the parameters are passed to a subroutine?

MODULE -3

1. With a neat diagram explain the internal organization of a 2Mx8 dynamic memory chip.
2. Explain associative mapping technique and set associative mapping technique.
3. What is virtual memory? With a diagram explain how virtual memory address is translated.
    i) Write a note on
    ii) Magnetic tape system
    iii) Flash memory
4. What is Stack? Explain its role in subroutine nesting.
5. For a DMA controller to be able to interrupt the processor?
6. What are the advantages do DMA and DMAC?.
7. Define following interrupt, vectored interrupt, interrupt nesting and an exception and give 2 examples.
8. Explain in brief with the help of diagram, the working principle of daisy chain with multiple priority levels and multiple devices in each level.
9. Explain I/O mapped I/o and describe any two methods of connecting multiple interrupting devices to CPU.
10. What is DMA? Explain the generation of two channel DMA controller

MODULE -4

1. Explain the internal organization of of 2M*8 dynamic memory chip.
2. Differentiate between SRAM and SDRAM chips
3. Define the following Memory access time, memory cycle time, RAM, static memories.
4. Differentiate between the static RAM and DRAM giving four key differences. State the primary usage of SRAM and DRAM in contemporary computer systems.
5. Define memory latency and bandwidth in case of burst operation that is used for transferring a block of data to or from synchronous DRAM memory unit.

MODULE -5

1. Draw and explain multiple bus organization of CPU, and write the control sequence for the instruction Add R4, R5, R6 for the multiple bus organization.
2. Explain with neat diagram, micro- programmed control method for design of control unit and write the micro – routine for the instruction Branch < 0.
3. With block diagram, explain parallel I/O interface.
4. Explain the fetching of word from memory with the help of timing diagram.
5. Compare between hardwired and micro-programmed control.
6. Sequence of control to perform the actions for single bus structure. Explain the steps.

15.0 University Result

Examination	S+	S	A	B	C	D	E	% Passing
New subject	0	5	17	9	3	--	--	100%
2020-21	0	2	13	14	--	--	1	96.67%

Prepared by	Checked by		
Prof. B. P. Khot	Prof. S. S. Kamate	HOD	Principal

Subject Title	**POWER ELECTRONICS & INSTRUMENTATION**		
Subject Code	18EC36	**CIE Marks**	40
Number of Lecture Hrs / Week	03	**SEE Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof . S. S. Ittannavar	**Designation:** Assistant Professor	**Experience:** 08.6 yrs
No. of times course taught:02	**Specialization:** Digital Signal Processing	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	I / II	Basic Electrical & Electronics

2.0 Course Objectives

This course will enable students to:

- Study and analysis of thyristor circuits with different triggering conditions.
- Learn the applications of power devices in controlled rectifiers, converters and inverters.
- Understand types of instrument errors.
- Develop circuits for multirange Ammeters and Voltmeters. Multimeters and
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operation of Transducers, Instrumentation amplifiers and PLCs.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	RBT Level	POs
C206.1	Build and test circuits using power devices.	L1 , L2	PO1,2,3,4,5,6,12
C206.2	Analyze and design controlled rectifier, DC to DC converters, DC to AC inverters and SMPS.	L1 , L2 , L3	PO1,2,3,4,5,6,12
C206.3	Analyze instrument characteristics and errors.	L1 , L2,L3	PO1,2,3,4,5,6,12
C206.4	Describe Principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.	L1 , L2	PO1,2,3,4,5,6,12
C206.5	Explain the principle, design and analyze the transducers for measuring physical parameters.	L1 , L2,L3	PO1,2,3,4,5,6,12
Total Hours of instruction		**40**	

4.0 Course Content

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: **Introduction:** History, Power Electronic Systems, Power Electronic Converters and Applications. **(1.2, 1.3, 1.5 & 1.6 of Text 1)** **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn- ON methods, Turn-OFF mechanisms(**2.3, 2.6 without 2.6.1), 2.7, 2.9 of text 1**), Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types (**refer 2.10 without design considerations**), Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit (**refer 3.5 up to 3.5.2 of Text 1**), Unijunction Transistor: Basic operation and UJT Firing Circuit (**refer 3.6, up to 3.6.4, except 3.6.2 of Text 1**).	**08 Hours**	**L1 , L2**
Module 2: **Phase Controlled Converter:** Control techniques, Single phase half wave and full wave controlled rectifier with resistive and inductive loads, effect of freewheeling diode (**refer Chapter 6 of Text 1 upto6.4.1 without derivations**). **Choppers:** Chopper Classification, Basic Chopper operation: step-down, step-up and step-up/down choppers. (**refer Chapter 8 of Text 1upto 8.3.3**)	**08 Hours**	**L1 , L2, L3**
Module 3: **Inverters:** Classification, Single phase Half bridge and full bridge inverters with R and RL load (**refer Chapter 9 of Text 1 up to 9.4.2 without Circuit Analysis**). **Switched Mode Power Supplies**: Isolated Flyback Converter, Isolated Forward Converter (**only refer to the circuit operations in section 16.3 of Text 1upto 16.3.2 except 16.3.1.3 and derivations**). **Principles of Measurement:** Static Characteristics, Error in Measurement, Types of Static Error. **(Text 2: 1.2-1.6)** Multirange Ammeters, Multirange voltmeter. **(Text 2: 3.2, 4.4)**	**08 Hours**	**L1 , L2,L3**
Module 4: Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM **(Text 2: 5.1-5.3, 5.5, 5.6)** **Digital Multimeter:** Digital Frequency Meter and Digital Measurement of Time, Function Generator. **Bridges:** Measurement of resistance: Wheatstone's Bridge, AC Bridges-Capacitance and Inductance Comparison bridge, Wien's bridge.**(Text 2: refer 6.2, 6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8, 11.2, 11.8-11.10, 11.14).**	**08 Hours**	**L1 , L2**
Module 5: **Transducers:** Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT. **(Text 2: 13.1-13.3, 13.5, 13.6 upto 13.6.1, 13.7, 13.8, 13.11).** Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale **(Text 2: 14.3.3, 14.4.1, 14.4.3).** **Programmable Logic Controller:** Structure, Operation, Relays and Registers **(Text 2: 21.15, 21.15.2, 21.15.3, 21.15.5, 21.15.6).**	**08 Hours**	**L1 , L2,L3**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	LIC, Verilog & Project work	Signal generators, digital instruments & transducers.

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Measuring and controlling instruments, display equipments.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial, Videos	Topic: transducers and digital instruments.

8.0 Books Used and Recommended to Students

Text Books
1. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897 2. H. S. Kalsi, "Electronic Instrumentation", McGraw Hill, 3rd Edition 2012, ISBN: 9780070702066.
Reference Books
1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5. 2. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009. 3. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2. 4. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN: 9789332556065.
Additional Study material & e-Books
3. NPTEL notes and Videos 4. VTU Online notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
04) https://nptel.co.in

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Explorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of three will be accounted for 30 Marks.
Assignment is10 Marks.
Total is 40 Marks

Scheme of Evaluation for Internal Assessment (50 Marks)
Four full questions will be given which consists of a, b as sub sections.
Students have to answer either Q: 1 or 2 and Q 3 or 4 completely.
Question 1 or 2 for 15 or 25Marks
Question 3 or 4 for 15 or 25Marks
Each IA will be conducted for 50 Marks.
Three IA will be conducted and average of three will be accounted for 30 Marks.
Assignment is 10 Marks
Total = 40Marks
Scheme of External Exam (60 Marks)
Ten questions to be set from the syllabus covered.
Each Module consists of two questions. Each question consists of a, b, c and d sub questions.
Student has to answer one full question from Each Module.
Each Module Consists of 20 Marks. Total 5 Modules=5*20=100 Marks
This 100 Marks results will be converted for 60 Marks.

12.0 Course Delivery Plan

Course Delivery Plan:

Module	Lecture No.	Content of Lecture	% of Portion
1	1	**Introduction :** History, Power Electronic Systems,	20
	2	Power Electronic Converters and Applications.	
	3	**Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR	
	4	Turn- ON methods, Turn-OFF mechanisms Turn-OFF Methods	
	5	Natural and Forced Commutation	
	6	Class A and Class B types	
	7	Gate Trigger Circuit	
	8	Resistance Firing Circuit	
	9	Resistance capacitance firing circuit	
	10	Uni junction Transistor: Basic operation and UJT Firing Circuit.	
2	11	Phase Controlled Converter : Control techniques	20
	12	Single phase half wave controlled rectifier with resistive loads	
	13	Single phase half wave controlled rectifier with Inductive loads	
	14	Single phase full wave controlled rectifier with resistive loads	
	15	Single phase full wave controlled rectifier with Inductive loads	
	16	Effect of freewheeling diode	
	17	**Choppers:** Chopper Classification,	
	18	Basic Chopper operation: step-down,	
	19	Step-up choppers	
	20	Step-up/down choppers	
	21	**Inverters:** Classification	

3	22	Single phase Half bridge	20
	23	Full bridge inverters with R and RL load	
	24	**Switched Mode Power Supplies**: Isolated Flyback Converter	
	25	Isolated Forward Converter	
	26	Principles of Measurement	
	27	Static Characteristics	
	28	Error in Measurement, Types of Static Errors	
	29	Multirange Ammeters	
	30	Multirange voltmeter	
4	31	Digital Voltmeter: Ramp Technique,	20
	32	Dual slope integrating Type DVM,	
	33	Direct Compensation type	
	34	Successive Approximations type DVM	
	35	Digital Multimeter.	
	36	Digital Frequency Meter and Digital Measurement of Time,	
	37	Function Generator.	
	38	Bridges: Measurement of resistance, Wheatstone's Bridge,	
	39	AC Bridges-Capacitance	
	40	Inductance Comparison bridge, Wien's bridge	
5	41	Transducers: Introduction, Electrical Transducer,	20
	42	Resistive Transducer, Resistive position Transducer,	
	43	Resistance Wire Strain Gauges	
	44	Resistance Thermometer,	
	45	Thermistor, LVDT.	
	46	Instrumentation Amplifier using Transducer Bridge,	
	47	Temperature indicators using Thermometer	
	48	Analog Weight Scale	
	49	PLC: Structure, Operation	
	50	Relays and Registers	

13.0 QUESTION BANK

Module-1

1) Name the power semiconductor devices along their circuit symbols and maximum ratings.
2) Explain the operation of SCR, in terms of two transistor model and derive anode current and gate currents relation. Discuss how small gate current can trigger a device into condition.
3) Enumerate applications of Power Electronics.
4) Explain the operation of self commutation by resonating load [class A] with a relevant circuit and waveforms.
5) What are gate triggering schemes? Explain with the circuit diagram and waveforms, now RC triggering circuit is turns on SCR's.

Module-2

1) Explain control strategies used to operate choppers.
2) Explain with the circuit diagram and waveforms the operation single phase half wave controlled rectifiers with resistive load.
3) Derive the expression for i) Average load voltage ii) RMS load voltage.
4) Explain the effect of freewheeling diode used in controlled rectifiers.
5) Explain with the circuit diagram and waveforms the operation of set up chopper.

Module-3

1) Define the terms: i) Instrument ii) Accuracy iii) Absolute error iv) Relative errors?
2) Explain the operation of single-phase half bridge inverter connected to RL load, with the help of circuit and waveforms.
3) What are inverters? Classify the inverters according to commutations and connections?
4) What are the static errors? Explain them in detail with examples.
5) A single phase half bridge inverter, has resistive load of R=3Ω and DC input voltage is Vdc = 50 volts. Calculate : i) RMS output voltage at fundamental frequency ii) the output power

Module-4

1) Explain how a simple AC Bridge circuit operates.
2) Derive the expression for unknown parameters of AC Bridge.
3) With the aid of diagram, explain the working of unbalanced wheat stone bridge and derive for Galvanometer current expression.
4) What are the advantages of digital instruments over analog instruments
5) With neat block diagram, explain the operating principle of a Ramp type DVM.

Module-5

1) Define transducers. What are the advantages of electrical transducers?
2) Explain with neat diagram the PLC structure.
3) Explain instrumentation amplifier using Transducer Bridge with the help of circuit diagram.
4) What are the features of Instrumentation amplifiers? How it differs from ordinary operational amplifier?
5) Describe the operation of resistive position transducer with constructional diagram and typical circuit used?

14.0 University Result

Examination	S+	S	A	B	C	D	E	% Passing
January 2020	00	00	03	12	13	06	00	100
January 2021	00	00	10	17	01	00	00	93.33

Prepared by	Checked by		
Prof. S. S. Ittannavar	Prof. S. B. Akkole	HOD	Principal

Subject Title	**Electronic Devices and Instrumentation Lab**		
Subject Code	18ECL37	**IA Marks**	40
Number of Lecture Hrs / Week	2Hr Tutorial + 2 Hrs Lab	**Exam Marks**	60
Total Number of Lecture Hrs	50	**Exam Hours**	03
CREDITS – 04			

FACULTY DETAILS:		
Name: Prof. D. M. Kumbhar	**Designation:** Asst. Professor	**Experience:** 14 Years
No. of times course taught: --02	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	Basic Electronics

2.0 Course Objectives

At the end of the Course the student will be able to get practical experience in design, assembly, testing and evaluation of

i. Understand the circuit schematic and its working.
ii. Study the characteristics of different electronic devices.
iii. Design and test simple electronic circuits as per the specifications using discrete electronic components.
iv. Familiarize with EDA software which can be used for electronic circuit simulation.

3.0 Course Outcomes

On the completion of this laboratory course, the students will be able to:

	Course Outcome	RBT Level	POs
C207.1	Understand the characteristics of various electronic devices and measurement of parameters.	L1, L2, L3	PO1,2,3,4,5,9,10,12
C207.2	Design and test simple electronic circuits.	L1, L2, L3	PO1,2,3,4,5,9,10,12
C207.3	Use of circuit simulation software for the implementation and characterization of electronic circuits and devices.	L1, L2, L3	PO1,2,3,4,5,9,10,12
Total Hours of instruction		**50**	

Conduct of Practical Examination:
All laboratory experiments are to be included for practical examination. Students are allowed to pick one experiment from the lot. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

4.0 Course Content

Laboratory Experiments:

S.N	Experiments	Revised Bloom's Taxonomy (RBT) Level
	PART A	
1	Conduct experiment to test diode clipping(single/double ended) and clamping circuits(positive/negative)	**L1,L2,L3**
2	Half wave Rectifier and Full wave Rectifier with and without filter and measure the ripple factor.	**L1,L2,L3**
3	Characteristics of Zener diode and design a simple Zener voltage regulator to determine line and load regulation.	**L1,L2,L3**

4	Characteristics of LDR and photodiode and to turn on an LED using LDR.	**L1,L2,L3**
5	Static Characteristics of SCR.	
6	SCR controlled HWR and FWR using RC triggering circuit.	**L1,L2,L3**
7	Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge.	**L1,L2,L3**
8	Measurement of Resistance using whetstone's bridge and Kelvin's bridge.	**L1,L2,L3**
PART B		
1	Input and output characteristics of BJT Emitter configuration and Evaluation of Parameters.	**L1,L2,L3**
2	Transfer and drain characteristics of a JFET and MOSFET.	**L1,L2,L3**
3	UJT triggering circuits for Controlled Rectifiers,.	**L1,L2,L3**
4	Design and simulation of Regulated Power supply.	**L1,L2,L3**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Electronics Devices based projects.
02	VI	Analog Circuits lab	Analog Electronics circuit lab

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analog Electronics based components
02	Design of rectifiers, Sensor applications and regulators.

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Rectifiers, Transducers, FET and Regulators
02	NPTEL	Electronic devices and circuits.

8.0 Books Used and Recommended to Students

Text Books
1. Analog Lab Manual by Nawas. 2. David A Bell ,Fundamentals of Electronics Devices and circuits Lab Manual",5 th Edition,2009 3. Muhammed H Rashid "Introduction to Pspice using ORcad for circuits and electronics"3 rd Edition.

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1) https://vtu.ac.in 2) http://www.bookspar.com/engineering-vtu 3) https://www.youtube.com/watch?v=Tnqi0JNWwTQ

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	Research gate	https://www.researchgate.net/publication/292140898_Performance_of_shunt_voltage_regulators_based_on_Zener_diodes_at_cryogenic_temperatures
2	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)

(a) Continuous Assessment 30 marks

(b) Internal Assessment test 10 marks

SCHEME OF EXAMINATION:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

12.0 Course Delivery Plan

Experiment	Content	% of Portion
1	Conduct experiment to test diode clipping(single/double ended) and clamping circuits(positive/negative)	7.14
2	Half wave Rectifier and Full wave Rectifier with and without filter and measure the ripple factor.	14.28
3	Characteristics of Zener diode and design a simple Zener voltage regulator to determine line and load regulation.	21.42
4	Characteristics of LDR and photodiode and to turn on an LED using LDR.	28.57
5	Static Characteristics of SCR.	35.71
6	SCR controlled HWR and FWR using RC triggering circuit.	42.85
7	Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge .	50
8	Measurement of Resistance using wheatstone's bridge and kelvin's bridge.	64.28
9	Input and output characteristics of BJT Emitter configuration and Evaluation of Parameters.	71.42
10	Transfer and drain characteristics of a JFET and MOSFET.	85.71
11	UJT triggering circuits for Controlled Rectifiers,.	92.85
12	Design and simulation of Regulated Power supply.	100

13.0 VIVA BANK

1. Explain how do you determine the forward and reverse resistance of a diode.
2. Draw the equivalent circuit for an ideal diode.
3. Draw the equivalent circuit for a practical diode.
4. Explain the working of diode rectifier circuits with & without filter.
5. What is ripple & Ripple factor.
6. What is clipping? What is Clamping?
7. What is meant by +ve Clipping & -ve Clipping.
8. What is meant by +ve clamping & -ve Clamping.
9. Explain anyone diode clipper circuit.
10. Explain anyone diode clamper circuit.
11. What is meant by biasing of a transistor?
12. Draw and explain the reverse characteristics of a Zener diode. Explain zener diode as voltage regulator.
13. Define rectification.
14. Define three stability factors.
15. Explain the need of cascading amplifiers.
16. What is positive feedback?
17. What is negative feedback?

18. What is filter?
19. Define Bridge. Explain the condition when bridge is balanced.
20. Explain the working principle of Whetstones bridge and Kelvin's bridge.
21. What are the advantages and disadvantages of center tapped full-wave rectifiers compared with Bridge rectifiers?
22. Define Ripple factor 'γ' and its values for the three types of rectifiers.
23. What is the value of No load voltage for all the three types of the rectifiers?
24. What are the different types of filters used for the rectifiers?
25. What is meant by Line Regulation & Load Regulation?
26 Explain the working principle and characteristics of LDR and Photodiode.
27. Explain the static characteristics of SCR.
28. Define Bridge. Explain the working principle of Whetstones Bridge and Kelvin's bridge.
29. Define Temperature sensor.
30 Define UJT.
31. Explain the input and output characteristics of BJT Emitter configuration and evaluation of parameters.
32. Define JFET and MOSFET. Draw the characteristics of JFET and MOSFET.

14.0 University result

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Examination	FCD	FC	SC	% Passing
March 2021	28	1	1	100

Prepared by	Checked by		
Prof. D. M. Kumbhar	Prof. S. B. Akkole	HOD	Principal

Subject Title	**DIGITAL SYSTEM DESIGN LAB**		
Subject Code	18ECL38	**CIE Marks**	40
Number of Lecture Hrs / Week	02 Hr Tutorial (Instructions) + 02 Hrs Laboratory = 04	**SEE Marks**	60
		Exam Hours	03
CREDITS – 02			

FACULTY DETAILS:		
Name: Prof. D. B. Madihalli	**Designation:** Asst. Professor	**Experience:** 14 years
No. of times course taught: 06	**Specialization:** Industrial Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	Basic Electronics
02	Electronics & Communication Engineering	III	Digital Electronics

2.0 Course Objectives

This course will enable students to get practical experience in design , realisation & verification of

- Demorgan's Theorem , SOP , POS forms.
- Full / Parallel Adders , Subtractors & Magnitude Comparator.
- Multiplexer using logic gates.
- Demultiplexers & Decoders.
- Flip-Flops , Shift registers & Counters.

3.0 Course Outcomes

At the end of the course students will be able to:

	Course Outcome	RBT Level	POs
C208.1	Design , realize and verify DeMorgan's theorems, SOP & POS forms	L1,L2,L3,L4	PO1,2,3,4,5,6,9,10,11,12.
C208.2	Demonstrate the truth table of various expressions & combinational circuits using logic gates.	L1,L2,L3,L4	PO1,2,3,4,5,6,9,10,11,12.
C208.3	Design various combinational circuits such as adders, sub tractors, comparators, multiplexers and demultiplexers.	L1,L2,L3,L4	PO1,2,3,4,5,6,9,10,11,12.
C208.4	Construct flip-flops, counters & shift registers.	L1,L2,L3,L4	PO1,2,3,4,5,6,9,10,11,12.
C208.5	Simulate serial adder & binary multiplier.	L1,L2,L3,L4	PO1,2,3,4,5,6,9,10,11,12.
Total Hours of instruction		**48**	

4.0 Course Content

Laboratory Experiments:

1	Verify (a) Demorgan's Theorem for 2 variables. (b) The sum -of product and product -of-sum expressions using universal gates.
2	Design and implement (a) Half Adder & Full Adder using (i) basic logic gates and (ii) NAND gates. (b) Half Subtractor & Full subtractor using (i) basic logic gates and (ii) NANAD gates
3	Design and implement of (a) 4-bit Parallel Adder/ Subtractor using IC 7483. (b) BCD to Excess-3 code conversion and vice versa.
4	Design and Implementation of (a) 1-bit Comparator. (b) 5-bit Magnitude Comparator using IC 7485.
5	Realize (a) Adder & Subtractors using IC 74153. (b) 4-variable function using IC 74151(8:1MUX).
6	Realize (a) Adder & Subtractors using IC74139. (b) Binary to Gray code conversion & vice versa (IC74139).
7	Realize the following flip/flops using NAND gates. Master-Slave JK, D & T Flip-Flop.
8	Realize the following shift registers using IC7474/IC 7495 (a)SISO (b) SIPO (c) PISO (d) PIPO (e) Ring and (f) Johnson counter.
9	Realize (i) Design Mod-N Synchronous Up counter & Down Counter using 7476 JK F/F. (ii) Mod-N Asynchronous Counter using IC7490/7476. (ii) Mod-N Synchronous counter using IC74192.
10	Design Pseudo Random Sequence generator using 7495.
11	Design serial adder with accumulator and simulate using simulation tool.
12	Design binary multiplier and simulate using simulation tool.

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Digital Electronics based projects

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Analyze different types of digital circuits in digital systems.
02	Design of adders , counters & multiplexers.

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Topic : Design of adders , counters & multiplexers.
02	NPTEL	Digital Electronics Circuits

8.0 Books Used and Recommended to Students

Text Books
1.Digital System Design Lab Manual

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
4) https://vtu.ac.in 5) http://www.bookspar.com/engineering-vtu 3) http://www.slideshare.net/farohalolya/digital electronics - lab-manual 4) https://www.youtube.com/results?search_query=digital electronics circuit

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)
(a) Continuous Assessment 30 marks.
(b) Internal Assessment Test 10 marks (Write Up = 1.5M, Conduction = 07M, Viva = 1.5M)
SCHEME OF EXAMINATION:
Two questions to be set. Student has to answer both full questions. 100 Marks divided in three parts 15M = Write up marks, 70M = Conduction marks & 15M = Viva marks.

12.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1	**1**	Verify (a) Demorgan's Theorem for 2 variables. (b) The sum -of product and product -of-sum expressions using universal gates.	7
2	**2**	Design and implement (a) Half Adder & Full Adder using (i) basic logic gates and (ii) NAND gates. (b) Half Subtractor & Full subtractor using (i) basic logic gates and (ii) NANAD gates	14
3	3	Design and implement of (a) 4-bit Parallel Adder/ Subtractor using IC 7483. (b) BCD to Excess-3 code conversion and vice versa.	21

4	4	Design and Implementation of (a) 1-bit Comparator. (b) 5-bit Magnitude Comparator using IC 7485.	29
5	**5**	Realize (a) Adder & Subtractors using IC 74153. (b) 4-variable function using IC 74151(8:1MUX).	36
6	6	Realize (a) Adder & Subtractors using IC74139. (b) Binary to Gray code conversion & vice versa (IC74139).	43
7	**7**	Realize the following flip/flops using NAND gates. Master-Slave JK, D & T Flip-Flop.	50
8	8	Realize the following shift registers using IC7474/IC 7495 (a)SISO (b) SIPO (c) PISO (d) PIPO (e) Ring and (f) Johnson counter.	64
9	9	Realize (i) Design Mod-N Synchronous Up counter & Down Counter using 7476 JK F/F. (ii) Mod-N Asynchronous Counter using IC7490/7476. (ii) Mod-N Synchronous counter using IC74192.	72
10	10	Design Pseudo Random Sequence generator using 7495.	86
11	11	Design serial adder with accumulator and simulate using simulation tool.	93
12	12	Design binary multiplier and simulate using simulation tool.	100

13.0 VIVA BANK

1. What is digital gate?
2. What is universal gate?
3. What is truth table?
4. What is the difference between Ex-OR and Ex-NOR gate.
5. What is demorgan's theorem?
6. What are demorgan's theorem equations?
7. What is the use of full adder?
8. In full adder , how many inputs are used.
9. In output of full adder what we gate.
10. What is the equation of SUM of full adder.
11. How many half adders are required to make full adder.
12. In full adder how many types of gates are required.
13. Draw the half adder diagram.
14. What is the difference between half & full adder.
15. Write the expression of CARRY of full adder.
16. Draw the diagram of half subtractor.
17. What is the difference between half & full subtractor.
18. What is magnitude comparator?
19. What is most significant bit ?

20. What is the operation of AND gate ?
21. What is the operation of comparator's truth table. ?
22. What is equality & inequality ?
23. What is 8 input magnitude comparator ?
24. What is IC ?
25. What is flipflop?
26. How many types of flipflop are used?
27. What is disadvantage of SR F/F?
28. What is disadvantage of JK F/F ?
29. To remove race around condition what we use?
30. What is race around condition?
31. What is the use of D F/F ?
32. What is multiplexer ?
33. What is demultiplexer ?
34. What is counter ?
35. What are the types of counter ?
36. What is ripple counter ?
37. What is Johnson counter ?
38. What is decade counter ?
39. What is synchronous counter ?
40. Write the truth table of 2 bit counter.
41. What is ring counter ?
42. How many stages are required for decade counter.
43. What causes specified condition to shift position.
44. What is shift register ?
45. What is clock enble ?
46. What is clock ?
47. What is serial adder ?
48. What is binary multiplier ?

14.0 University Result

Examination	S+	S	A	B	C	D	E	F	% Passing
Dec-2019/Jan-20120	13	12	04	03	05	03	00	00	100
Dec-2020/Jan-2021	22	08	00	00	00	00	00	00	100

Prepared by	Checked by		
Prof. D.B.Madihalli	Prof. S. B. Akkole	HOD	Principal